

Optimum Harmonic Reduction with a Wide Range of Modulation Indexes for Multilevel Converters

Siroj Sirisukprasert*, Jih-Sheng Lai
Virginia Polytechnic Institute and State University
Center for Power Electronics Systems (CPES**)
665 Whittemore Hall
Blacksburg, VA 24061-0111

Tian-Hua Liu
National Taiwan University of Science and Technology
43 Keelung Road, Section 4
Taipei, Taiwan

Abstract - This paper proposes a novel modulation technique applying in multilevel voltage source converters suitable for high voltage power supplies and flexible ac transmission system (FACTS) devices. The proposed technique can generate output stepped-waveforms with a wide range of modulation indexes and minimized total voltage harmonic distortion. The main power devices switch only one time per cycle, suitable for high power applications. For the proposed harmonic reduction technique, the theoretical analysis is presented. By using a systematic method, only the polarities and the number of levels are required to be determined for different modulation levels. Computer simulation results are then provided. To verify the theory and the simulation results, a cascade inverter based hardware prototype including a low cost 8-bit microcontroller and modularized power stage and gate driver circuits, is implemented. Experimental results indicate that the proposed technique is effective for harmonic reduction in multilevel converters, and that both theoretical and simulation results are well validated.

I. INTRODUCTION

Recently, multilevel voltage source converters become an important technology in high power applications. Several multilevel converter topologies [1-4] and modulation techniques [5-8] have been developed and applied in high power systems. With devices or converter modules in series and with balanced voltage sharing among them, the lower voltage-rated switches can be possibly used in high voltage multilevel converter. With the requirement of the quality and efficiency in a high power system and the limitation of high power device switching speed, low switching frequency and small total harmonic distortion (THD) are desirable. By applying appropriate modulation schemes, these two goals can be achieved simultaneously. Challenge of the modulation techniques, therefore, plays a very important role in multilevel converter circuits.

The harmonic optimization techniques in [3] and [6] initiate the concept of achieving harmonic reduction with selected harmonic elimination. These techniques require more than one switching per cycle to obtain a wide modulation index. In this paper, the proposed modulation

technique is to generalize the optimum harmonic reduction technique that switches the main power devices one time per cycle and at the same time, achieves a wide range of modulation indexes. The output voltage presents stepped-type wave shape, similar to what can be achieved with the traditional methods. This method is fairly simple to implement in multilevel converters. The basic concept is to swap the polarity of some levels so that a low modulation index can be obtained. The computation effort is seamless for the entire range of modulation indexes. Consider for a seven-level cascade inverter. The traditional selected harmonic elimination can only achieve down to 0.5. The proposed method, however, indicates 0.1 can be easily achieved.

II. OPTIMIZED HARMONIC STEPPED-WAVEFORM TECHNIQUE

A. Conventional Stepped-Waveforms

Fig. 1 shows a generalized quarter-wave symmetric stepped voltage waveform synthesized by a $2m+1$ level converter, where m is the number of switching angles. By applying Fourier Series, the amplitude of any odd n^{th} harmonic of the stepped-waveform can be expressed as (1), whereas the amplitudes of all even harmonics are zero.

$$h_n = \frac{4}{n\pi} \sum_{k=1}^m [V_k \cos(n\alpha_k)] \quad (1)$$

where V_k is the k^{th} level dc voltage.
 n is an odd harmonic order.
 m is the number of switching angles.
and α_k is the k^{th} switching angle.

According to Fig. 1, α_1 to α_m must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \dots < \alpha_m < \frac{\pi}{2}.$$

Consider (1). To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $m-1$ harmonic components can be removed from the voltage waveform. In general, the most significant low frequency harmonic components will be chosen to eliminate. Then, high frequency harmonic components can be readily

* Supported by The Royal Thai Government

** This work made use of ERC Shared Facilities supported by the National Science Foundation under award EEC-9731677

removed by using additional filter circuits. According to (1), to keep the number of eliminated harmonics as constant, all switching angles must be less than $\pi/2$. However, if the switching angles do not satisfy the condition, this scheme is no longer exist. As a result, this modulation scheme basically provides a narrow range of modulation index, which is the main disadvantage. For example, in a seven-level equally stepped-waveform, its modulation index is only available from 0.5 to 1.05. At modulation index lower than 0.5, if this scheme is still applied, the possibly eliminated harmonic components will reduce from 2 to 1. The total voltage harmonic distortion in turn increases.

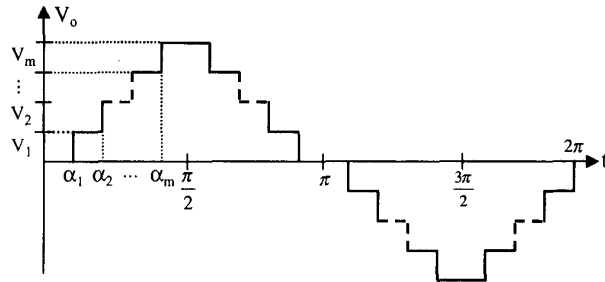


Fig. 1. Generalized $2m+1$ level quarter-wave stepped voltage waveform.

B. New Stepped-Waveforms

As discuss above, the traditional stepped-waveform provides a narrow modulation index range. This paper, therefore, proposes a new modulation technique, which can generate output voltage waveforms with a wide range of modulation indexes. With appropriated switching angles, this proposed modulation scheme also minimizes THD of the synthesized waveforms. To minimize the THD of line voltage, the lowest significant $m-1$ non-triplen harmonic components need to be eliminated from the synthesized phase voltage. Take a three-phase seven-level stepped-waveform as an example. In this case, m equals 3. To minimize line-to-line voltage harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to two surplus harmonics can be removed. Thus, the 5th and 7th harmonics, the two lowest non-triplen harmonics, are chosen to be eliminated from the phase voltages.

The new stepped-waveform concept, which provides a wide range of modulation indexes and remains the number of eliminated harmonic components, is proposed in this section. Fig. 2 illustrates the positive half cycle of seven-level stepped-waveforms with different modulation index levels. In this case, the range of modulation indexes can be divided into three levels such as high, middle, and low level. An output waveform with high modulation index level is shown in Fig. 2(a). Whenever α_3 is greater than $\pi/2$, this waveform is no longer exist. Therefore, an output waveform shown in Fig. 2(b), which gives middle modulation index level, will be

applied instead. When the switching angles α_1 to α_3 in Fig. 2(b) are not convergent at low modulation index level, an output waveform shown in Fig. 2(c) will replace. In general, a stepped-waveform, which comprises m switching angles, can be divided into m modulation index levels. By using this technique, low switching frequency and optimized harmonic in output waveforms with wide modulation index, can be achieved.

III. OPTIMUM HARMONIC REDUCTION WITH A WIDE RANGE OF MODULATION INDEXES IN $2M+1$ LEVEL WAVEFORM

By using Fourier Series, the odd harmonics of the waveforms shown in Fig. 2(a) to 2(c) are expressed as (2) to (4), respectively.

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2) + V_3 \cos(n\alpha_3)] \quad (2)$$

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2) - V_3 \cos(n\alpha_3)] \quad (3)$$

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) - V_2 \cos(n\alpha_2) + V_3 \cos(n\alpha_3)] \quad (4)$$

According to (2) through (4), α_1 through α_3 must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}.$$

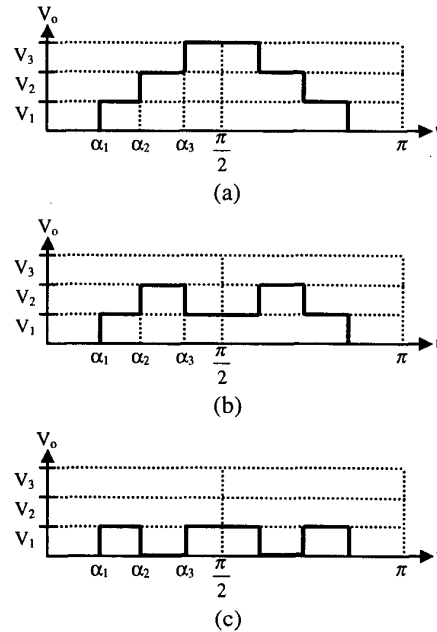


Fig. 2. A positive half cycle of a seven-level stepped-waveform with different modulation indexes (a) High modulation index (b) Middle modulation index (c) Low modulation index.

Because of symmetric characteristic, no even harmonic components exist in these three waveforms. By inspecting (2) to (4) and Fig. 2, at an edge corresponding to a switching angle, the rising edge provides positive polarity for the corresponding cosine term, whereas the falling edge gives the cosine term a negative polarity.

By observation, the generalized amplitude of harmonic components in $2m+1$ level output waveform for all modulation indexes is simply given as

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) \pm V_2 \cos(n\alpha_2) \pm \dots \pm V_m \cos(n\alpha_m)]. \quad (5)$$

where V_1 to V_m are the dc voltages at different levels.

n is an odd harmonic order.

m is the number of switching angles.

and α_1 to α_m are the switching angles and must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \dots < \alpha_m < \frac{\pi}{2}.$$

In (5), the positive sign expresses the rising edge and the negative sign expresses the falling edge. In this paper, V_1 to V_m are set to equal V_{dc} ; therefore, (5) becomes:

$$h_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) \pm \cos(n\alpha_2) \pm \dots \pm \cos(n\alpha_m)]. \quad (6)$$

By using systematic analysis, only the polarities and the number of levels are required to determine the switching angles for different modulation index levels in any multilevel topologies in which multilevel synchronous modulation is applied.

IV. SIMULATION RESULTS AND EXPERIMENTAL RESULTS

In this paper, a seven-level cascaded inverter system, which is shown in Fig. 3, is studied. Basically, the modulation index for cascade multilevel waveform, M , is defined as follows:

$$M = \frac{h_1}{mV_{dc}}. \quad (7)$$

where h_1 is the amplitude of the fundamental component.

m is the number of the switching angles.

and V_{dc} is the voltage of each dc source.

By using the Newton-Raphson method with (6) and (7), the switching angles for a given modulation index can be easily solved [6,9]. A seven-level waveform is used as an example. To minimize total line voltage harmonic distortion, the 5th and the 7th harmonics need to be eliminated from the

phase voltage. Thus, a set of nonlinear equations for $M = 0.4$, which is in middle modulation level, are given as follows:

$$[\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3)] = \frac{3(0.4)\pi}{4}. \quad (8)$$

$$[\cos(5\alpha_1) + \cos(5\alpha_2) - \cos(5\alpha_3)] = 0. \quad (9)$$

$$[\cos(7\alpha_1) + \cos(7\alpha_2) - \cos(7\alpha_3)] = 0. \quad (10)$$

To obtain the solution for these nonlinear equations, the Newton-Raphson method is applied. Likewise, the switching angles for other modulation indexes can be solved and are partially tabulated in Table 1. In this paper, total line voltage harmonic distortion is defined in (11).

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{200} [h_n]^2}}{h_1}. \quad (11)$$

where h_n is the amplitude of the n^{th} harmonic voltage.

h_1 is the amplitude of the fundamental voltage.

TABLE I
CALCULATED SWITCHING ANGLES FOR DIFFERENT MODULATION INDEX LEVEL

Modulation index level	Modulation index, M	α_1	α_2	α_3
High M	1.0	11.68°	31.18°	58.58°
	0.85	22.77°	49.38°	64.57°
Middle M	0.4	44.17°	74.33°	87.40°
Low M	0.1	55.85°	63.43°	83.02°

Fig. 4 shows the relationship between the entire modulation indexes and the calculated line voltage THD. From Fig.4, we can observe that the line voltage THD is inversely proportional to the modulation index. It is possible to reduce voltage THD at low modulation index; however, the proposed technique needs to be extended with more than one switching per cycle.

To verify the simulation results, a seven-level voltage source converter using cascaded-inverters with separated DC sources as shown in Fig. 3, is used as a hardware prototype. In a power stage, four IGBT, HGT30M60B model, are used as the main switches, which are connected in full-bridge configuration. Each power stage is supplied by a variable dc source. In the control circuit, an eight-bit microcontroller is employed to generate necessary gate drive signals. Fig. 5 shows simulation and experimental results of phase voltage, line voltage, and load current with the modulation index of 1.0, 0.85, 0.4, and 0.1. The experimental line voltage spectra in dB are also presented in Fig. 6. As expected, the results show that the 5th and the 7th harmonics of the line voltage are very small in magnitudes. Because of 120 degree phase shift

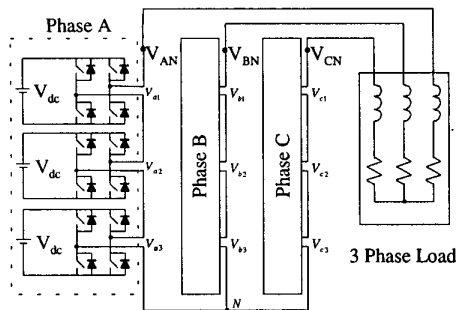


Fig. 3. A seven-level cascaded inverter system.

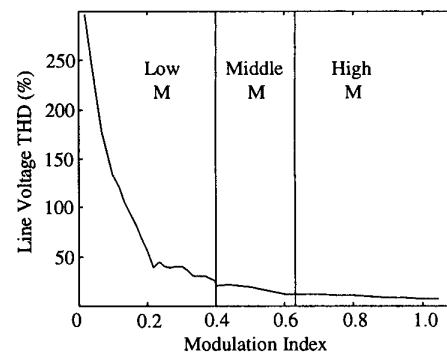
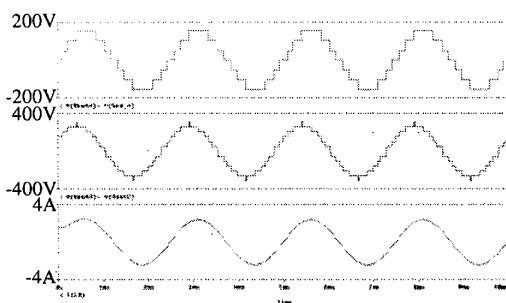
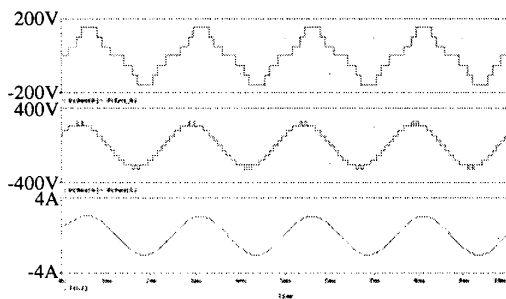


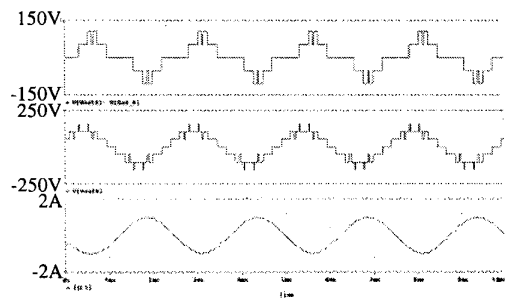
Fig. 4. Modulation index vs. line voltage THD.



$M = 1.0, \alpha_1 = 11.68^\circ, \alpha_2 = 31.18^\circ, \alpha_3 = 58.58^\circ$

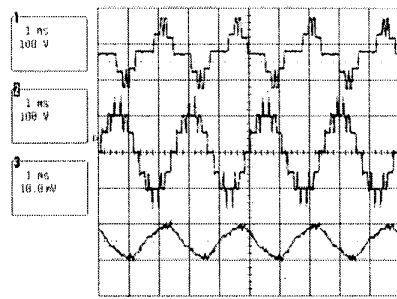
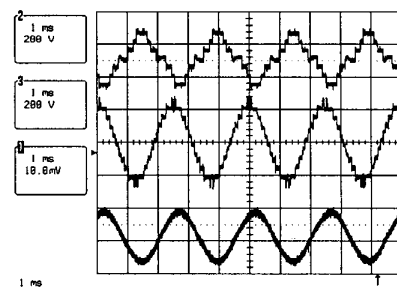
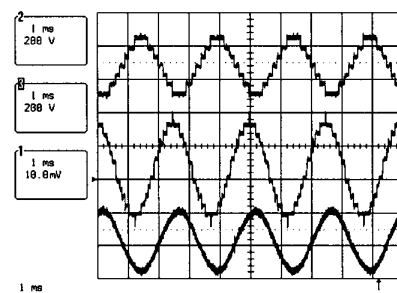


$M = 0.85, \alpha_1 = 22.77^\circ, \alpha_2 = 49.38^\circ, \alpha_3 = 64.57^\circ$



$M = 0.4, \alpha_1 = 44.17^\circ, \alpha_2 = 74.33^\circ, \alpha_3 = 87.40^\circ$

(a)



(b)

Fig. 5. The waveforms of phase voltage, line voltage, and load current
(a) Simulation results (b) Experimental results.

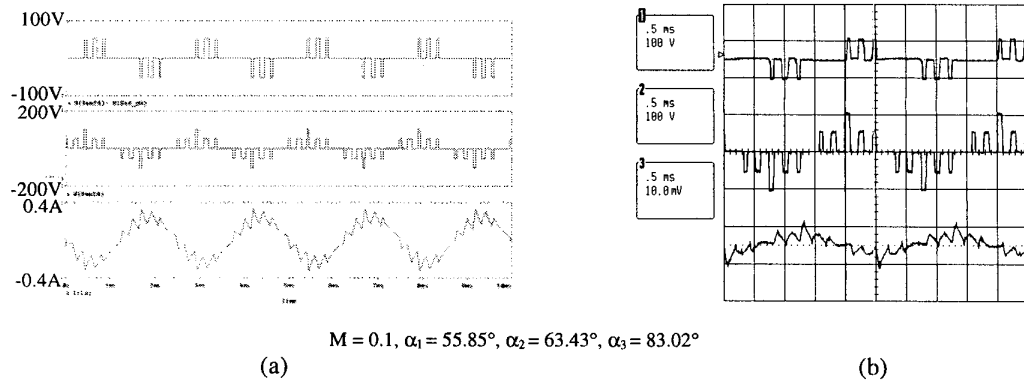


Fig. 5. (Cont.) The waveforms of phase voltage, line voltage, and load current
(a) Simulation results (b) Experimental results.

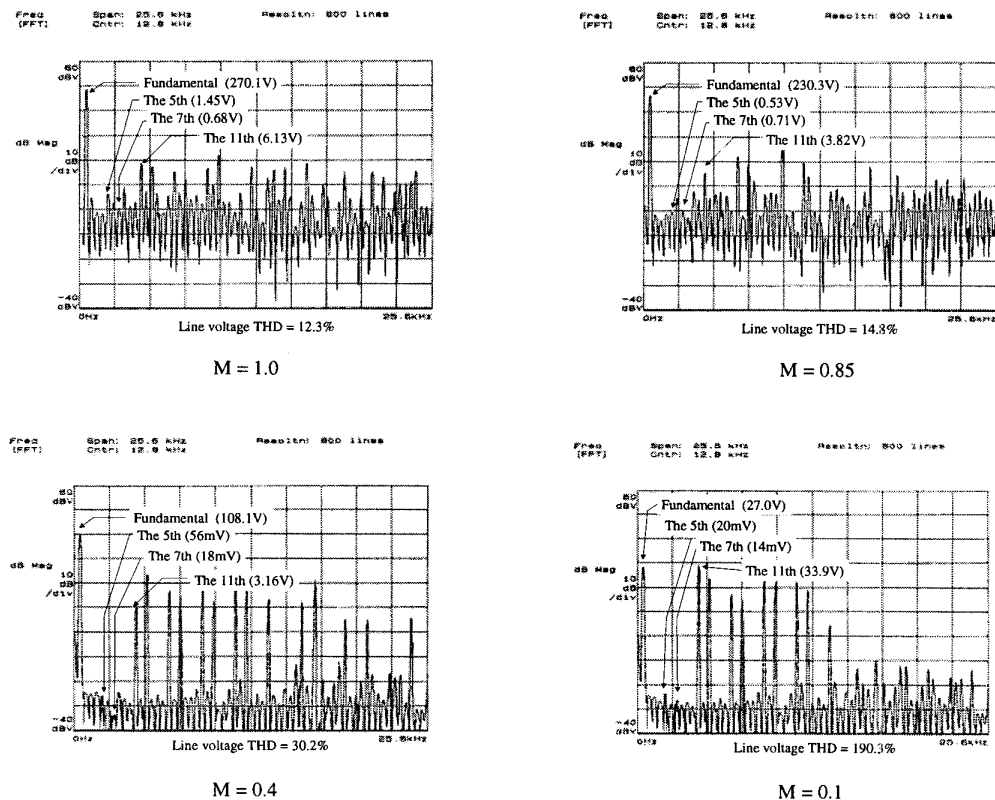


Fig. 6. The measured line voltage spectra.

among phase voltages, all triplen harmonics in line voltages are also very small. The experimental results match with the calculated and simulated results well.

Due to limited computational capability and control resolution, the experimental output quality is not as good as

expected, especially at low modulation indexes. It should be noted that the level of steps is actually reduced when modulation is less than 0.5. This results agrees the finding in initial analysis in which the convergence fails at $M = 0.5$. At $M = 0.4$, the 7 level becomes 5 levels, and at $M = 0.1$, it becomes 3 levels.

V. CONCLUSIONS

This paper presents a new modulation technique applying to multilevel voltage source converters suitable for high voltage high power applications. The proposed technique can generate output stepped-waveforms with wide modulation indexes, as well as minimum total harmonic distortion. For all modulation index levels, the switching devices of the main power stage switch only one time per cycle, which is suitable with the use of high power semiconductor devices. The simulation and experimental results validate the theoretical analysis with reasonable agreement. A three-phase seven-level cascaded inverter prototype is used as an example. The principle developed in this paper can be easily applied to other multilevel converter topologies and for any number of levels. For THD concern, the proposed technique can be further extended to have more than one switching per line cycle to lower THD at low modulation indexes.

REFERENCES

- [1] F. Z. Peng, J-S Lai, "Multilevel Converters – A New Breed of Power Converters," *IEEE Trans. on Ind. Appl.*, Vol.32, No.3, May/June, 1996, pp.509-517.
- [2] A. Nabae, I. Takahashi, H. Agaki, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. on Ind. Appl.* Vol.1A-17, No.5, Sep./Oct., 1981, pp.518-523.
- [3] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Trans. on Ind. Appl.*, Vol.1A-19, No.6 Nov./Dec., 1983, pp.1057-1069.
- [4] M. Carpita, S. Teconi, "A Novel Multilevel Structure for Voltage Source Inverter," in *Proc. EPE 1991*, pp. 90-94.
- [5] S. R. Bowes, "New Sinusoidal Pulse width-Modulated Inverter," in *Proc. IEE*, Vol.122, No.11, Nov, 1975.
- [6] H. S. Patel, R. G. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverter: Part I-Harmonic Elimination," *IEEE Trans. on Ind. Appl.*, Vol.1A.9, No.3, May/Jun., 1973, pp.310-317.
- [7] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis," in *Proc. IEEE Power Electron. Specialist Conf. (PESC)*, June, 1990, pp.363-371.
- [8] I. J. Pitel, S. N. Talukdar, P. Wood, "Characterization of Programmed-Waveform Pulsewidth Modulation," *IEEE Trans. on Ind. Appl.*, Vol.1A-16, No.5, Sep./Oct., 1980, pp.707-715.
- [9] J. Sun, H. Grotstollen, "Solving Nonlinear Equations for Selective Harmonic Eliminated PWM Using Predicted Initial Values," in *Proc. IECON 1992*, pp.259-264.
- [10] H. Johan, Frederik S. Van Der Merwe, "Voltage Harmonics Generated by Voltage-Fed Inverters Using PWM Natural Sampling," in *IEEE Trans. on Pow. Electron.*, Vol.3, July, 1988, pp.297-302.
- [11] F. Z. Peng, J. S. Lai, "Dynamic Performance and Control of a Static Var Generator Using Cascade Multilevel Inverters," *IEEE Trans. on Ind. Appl.*, Vol.33, No.3, May/June, 1997, pp.748-755.
- [12] L. M. Tolbert, F. Z. Peng, "Multilevel Converters for Large Electric Drives," *IEEE Trans. on Ind. Appl.*, Vol.35, No.1, Jan/Feb, 1999, pp. 36-34.
- [13] R. W. Menzies, P. Steimer, J. K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives," *IEEE Trans. on Ind. Appl.*, Vol.30, No.4, Jul./Aug., 1994, pp.938-944.