A Novel Multicell DC–AC Converter for Applications in Renewable Energy Systems

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***Abstract*—This paper presents a novel dc–ac converter for applications in the area of distributed energy generation systems, e.g., solar power systems, fuel-cell power systems in combination with supercapacitor or battery energy storage. The proposed converter is realized using an isolated multicell topology where the total ac output of the system is formed by series connection of several full-bridge converter stages. The dc links of the full bridges are supplied by individual dc-dc isolation stages which are arranged in parallel concerning the dc input of the total system. Therefore, all switching cells of the proposed converter can be equipped with modern low-voltage high-current power MOSFETs, which results in an improved efficiency as compared to conventional isolated dc–ac converters. Furthermore, the cells are operated in an interleaved pulsewidth-modulation mode which, in connection with the low voltage level of each cell, significantly reduces the filtering effort on the ac output of the overall system. The paper describes the operating principle, analyzes the fundamental relationships which are relevant for component selection, and presents a specific circuit design. Finally, measurements taken from a 2-kW laboratory model are presented.**

***Index Terms*—Interleaved pulsewidth modulation, multicell, renewable energy converter, solar inverter.**

I. Introduction

In CONNECTION with distributed energy generation and renewable energy sources (e.g., solar-cell or fuel-cell applications having battery or supercapacitor backup), in general, unidirectional and/or bidirectional dc–ac converters are applied frequently [1], [2]. To give an example, specific operating parameters and requirements of solar-power converters for typical residential applications should be summarized as follows: dc input voltage: 50–200 V; rated power: 500 W–2 kVA; ac output voltage (mains): 230 V_{RMS}; four-quadrant-operation of the dc–ac converter stage (generation of reactive power for stand-alone applications); and isolated topology (isolation between dc input and ac output due to safety requirements). Converter systems for the applications mentioned have to be designed considering very high efficiency and reliability. Frequently, circuit topologies using line-frequency transformers for isolation and voltage adaptation are applied. This results in high reliability because no semiconductor devices are connected directly to the mains and the transformer acts as an additional filtering stage. Fig. 1(a) shows a system based on a full-bridge topology as proposed, e.g., in [1] and [3] for three-phase applications. Alternatively, systems are known which rely on a center-tapped line-frequency isolation transformer and current shaping using a buck converter [4]. For unidirectional three-phase systems, the application of a line-frequency transformer gives an interesting possibility to achieve sinusoidal mains currents using two buck converters in connection with a thyristor bridge [5]. Furthermore, resonant topologies have also been proposed in order to improve the efficiency of the dc-to-ac conversion [6]. Of course, the dc-to-ac stage of Fig. 1(a) (i.e., the MOSFET full bridge) is itself already characterized by high efficiency because the relevant dc voltage levels in many cases allow the application of power transistors with ultralow on resistance (e.g., trench devices). The significant drawback of all topologies using a line-frequency transformer, however, is given by the impact of the transformer on the total efficiency and on the weight of the system. The efficiency of line-frequency transformers for the relevant power level is hardly better than 95% and, hence, the efficiency of the total system typically is only about 90%–92%.

In order to avoid the bulky mains transformer and/or to increase power density and efficiency, alternatively, topologies with high-frequency isolation based on a dc–dc system feeding the dc link of a full-bridge dc–ac converter connected directly to the mains are proposed [1], [7] [see Fig. 1(b)]. However, here, the low losses of the high-frequency isolation transformer have to be seen considering the additional losses of the rectifier stage and, especially, the line-side inverter. According to the required dc-link voltage level (e.g., 400 V), this power stage, in general, has to be equipped with insulated gate bipolar transistors (IGBTs), which show a nonoptimum efficiency for operating in the partial load area.

Remark: For equal losses at the rated operating point power MOSFETs showing resistive on-state behavior are more efficient as compared to IGBTs which show a more constant and/or current independent on-state voltage drop ($p_{\mathrm{on}} \approx R_{DS,\mathrm{on}} \cdot i_D^2$ for MOSFETs versus $p_{\mathrm{on}} \approx U_{CE,\mathrm{on}} \cdot i_C$ for IGBTs).

Consequently, considering the efficiency, the systems of Fig. 1 are about equivalent. The advantage of the topology of Fig. 1(b) is the increased power density due to the high-frequency isolation transformer. Furthermore, both systems of Fig. 1 are characterized by a single-stage ac voltage generation. This results in a poor mains current harmonic behavior, or, if the switching frequency is increased to lower the current harmonics, in a reduced efficiency.

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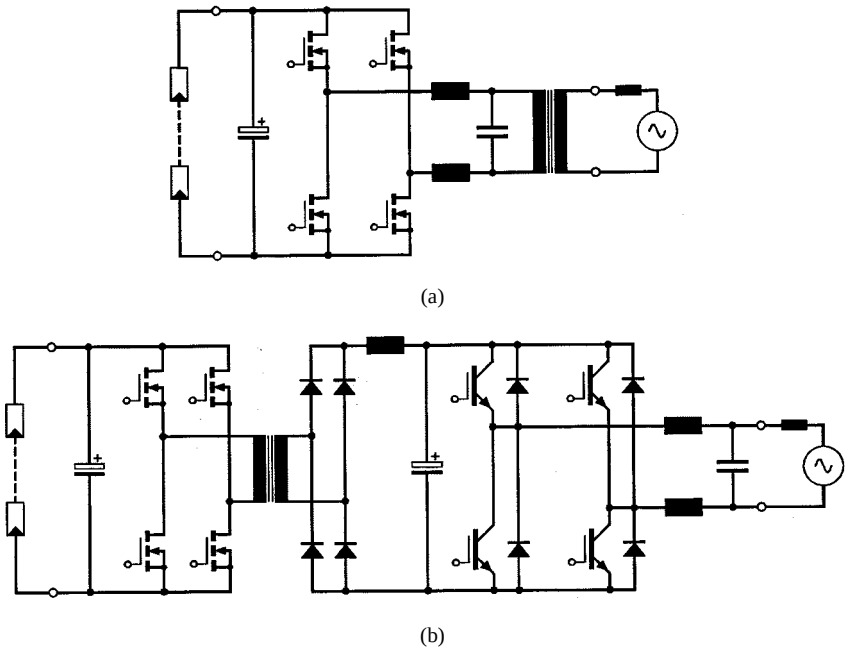


Fig. 1. Basic circuit topology of a solar-powered converter with (a) MOSFET full-bridge and line-frequency isolation transformer and, alternatively, (b) topology with MOSFET dc-dc converter (high-frequency isolation transformer) with subsequent single-cell IGBT four-quadrant dc–ac converter.

II. Multicell Converter—Basic Concept

Influenced by the recent developments in the area of low-voltage power MOSFETs, a converter topology is proposed for the application in residential renewable energy systems which originally is known from high-power applications. Multicell multilevel converter systems have been well known for many years for high-voltage/high-power applications in order to reduce the required blocking voltage of the power semiconductor devices. For example, fully static 50 Hz-to-16 2/3 Hz inverters for feeding railway overhead lines [8], converters for input current shaping and traction of locomotives [9], in general, for feeding medium- and high-voltage induction machines [10]–[12], as well as for static var compensators [13], [14], and also as a utility interface for medium-power renewable energy systems [15] have been reported.

Considering modern low-voltage power MOSFETs and integrated gate driver stages, however, multicell topologies have become attractive, even for converters in the lower power region. The applicability of low-cost standard power components designed for high-volume applications (automotive, telecommunication, etc.) overcomes the main drawback of such systems, i.e., the high number of switching devices. By application of multilevel multicell topologies, the drawbacks of the converter structures discussed in Section I can be avoided, resulting in compact units with high overall efficiency. There, the key specifications of the developed residential converter system are as follows:

dc input voltage $U_1 = 100$ V (80–120 V);
ac output voltage $U_{\mathrm{AC}} = 230\ V_{\mathrm{rms}}$;
rated power $P_N = 2$ kW;
efficiency $\eta > 94\%$ at rated power;
high-frequency isolation stage;
low-voltage MOSFETs (majority carrier devices).

According to Fig. 2, the total circuit is formed by multiple converter cells which are arranged in parallel on the dc input side and are connected in series for generating the ac output voltage. Each cell consists of a high-frequency isolation stage feeding the dc voltage link of a full-bridge inverter. Because of the series arrangement the inverter stages can also be realized in the same semiconductor technology as the isolation stages (i.e., application of low-voltage devices).

The isolation stage is implemented using a capacitively coupled half-bridge converter operated in a constant-frequency series-resonant mode [no pulsewidth modulation (PWM)] (see Section III). This results in low on-state losses (no freewheeling states) and low switching losses (zero-current and zero-voltage turn-on) for continuous conduction mode at switching frequencies being higher than the natural frequency of the resonant network. Consequently, the dc-link voltage of each dc–ac stage varies directly according to the dc input voltage of the total system.

The control of the ac output voltage/current is achieved by PWM of the dc–ac stages. As described in Section IV, this can be performed advantageously in an interleaved PWM mode of the individual cells in order to minimize the filtering effort. This is due to the fact that the resulting multilevel total output voltage of all cells then very closely approximates the sinusoidal voltage reference value. Therefore, the PWM switching frequency of each dc–ac cell can be chosen comparatively low, which results in low switching losses. Furthermore, it is advantageous to also operate the isolation stages in an interleaved manner in order to minimize the ripple current stress of the dc input smoothing capacitor.

III. Series-Resonant Isolation Stage

As mentioned before, the series-resonant topology has been chosen for the isolation stage due to the expected good efficiency based on the zero-current and zero-voltage turn-on of the power transistors. Furthermore, the blocking voltage stress on all semiconductors is well defined and the leakage of the

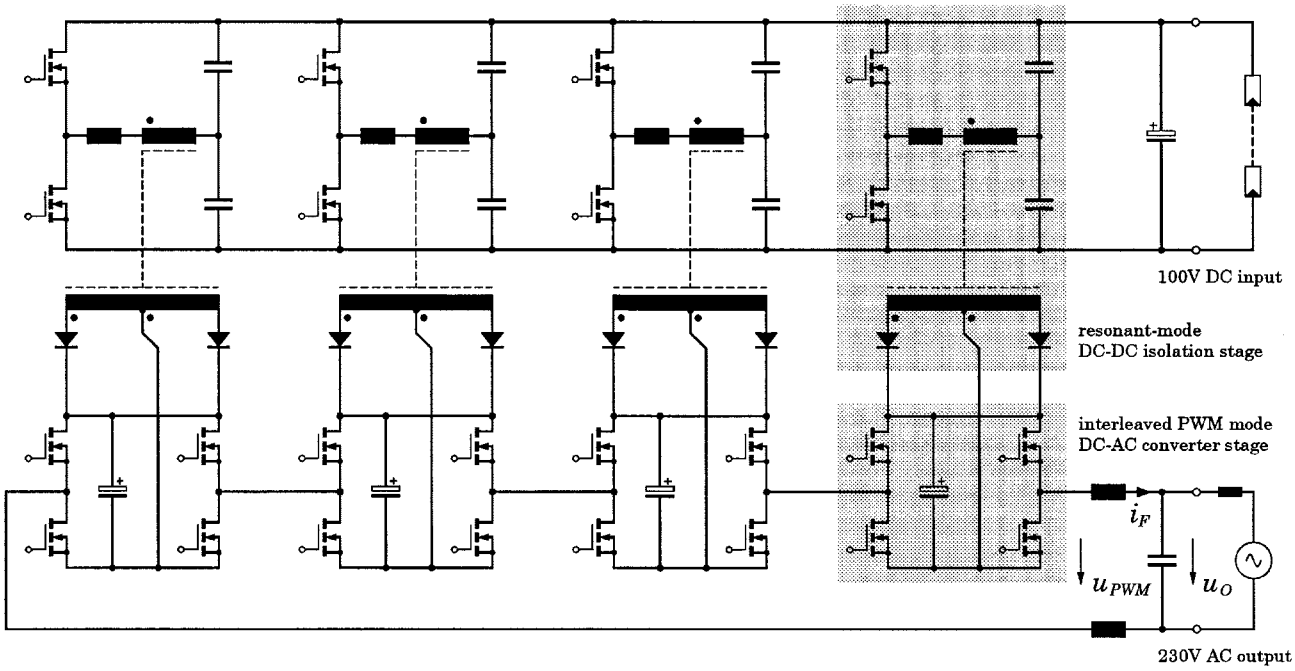


Fig. 2. Basic circuit topology of the proposed dc–ac multicell converter based on high-frequency resonant-mode dc–dc isolation stages feeding interleaved PWM-mode MOSFET dc–ac cells connected in series on the ac output ($N = 4$ cells).

transformer contributes to the effective inductance of the resonant network [16]. Therefore, different from, for example, transformers for flyback converters, a certain amount of leakage is desirable here. This is also of importance because the coupling capacitance between primary and secondary should be minimized because the proposed multilevel topology is characterized by a common-mode voltage stress of the converter cells caused by the interleaved switching of the individual dc–ac converter cells; a low coupling capacitance helps to reduce the resulting common-mode current. A circuit topology which is not sensitive to transformer leakage is furthermore of advantage because the primary winding of the transformer shall be realized by application of the "bow winding principle," i.e., copper wire bows are connected via the printed circuit board (PCB) to form the primary winding, whereas the secondary windings are of conventional type. Such a transformer usually shows significant leakage (but low coupling capacitance) and, therefore, is well suited for this series mode resonant topology.

A. Analysis of the Stationary Operating Behavior

In the following, the characteristics of the stationary operation shall be calculated analytically. It should be mentioned that a center-tapped secondary winding is used for the designed converter, which results in having only a single diode forward voltage drop as compared to bridge rectification [Fig. 3(a)].

Remark: For the desired output voltage range of up to 120 V, usually, 400-V diodes would be suitable for center-tapped rectification, whereas for bridge rectification 200-V diodes would be sufficient. Although 400-V devices show a higher on-state voltage than 200-V diodes, the two 200-V devices acting in series for bridge rectification cannot compete with the single 400-V diode of a center-tapped system.

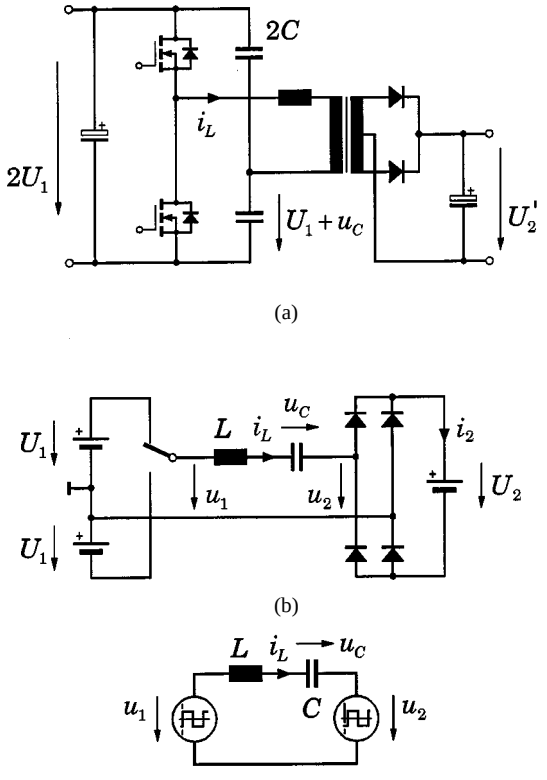


Fig. 3. Circuit diagram of the (a) series-resonant converter and (b), (c) corresponding equivalent circuits.

Here, the bridge rectifier is given only to develop the equivalent circuit diagrams of Fig. 3(b) and (c). The system is characterized by four different states defined by the polarities of the input voltage u_1 and of the reflected secondary voltage u_2. Whereas the polarity of u_1 is defined by the control circuit, the

TABLE I
OPERATING STATES OF THE SERIES-RESONANT CONVERTER

	$u_1 > 0$	$u_1 < 0$
$i_L > 0$	Ⓐ $\Delta U = U_1 - U_2$	Ⓑ $U_1 + U_2$
$i_L < 0$	Ⓓ $U_1 + U_2$	Ⓒ $\Delta U = U_1 - U_2$

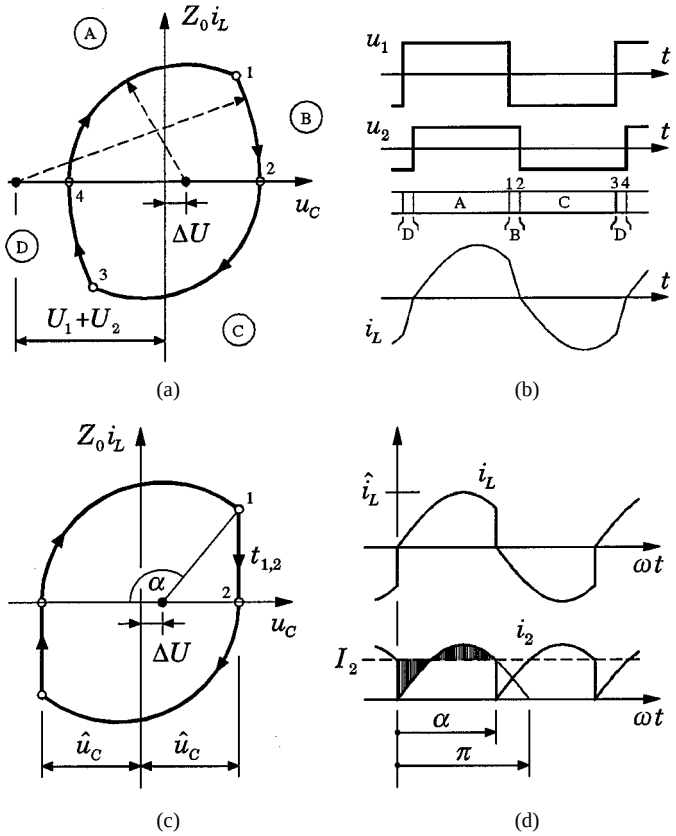


Fig. 4. (a) System trajectory and (b) time behavior of the series-resonant converter. (c), (d) Simplifications valid for $\Delta U \ll U_1$; i_2: output current of the rectifier [see Fig. 3(b)].

polarity of u_2 is given by the direction of the resonant current i_L. The four possible states (A $\rightarrow$ B $\rightarrow$ C $\rightarrow$ D) are listed in Table I. For state A, voltages u_1 and u_2 show equal direction and the (small) difference $\Delta U = U_1 - U_2$ is applied to the *LC* series circuit. This results in a circular-shaped system trajectory around the center point $[+\Delta U, 0]$ (see the $u_C - Z_0 i_L$ diagram in Fig. 4(a), $Z_0 = \sqrt{L/C}$ defines the characteristic impedance of the resonant network). Because the system operates with a switching frequency f_S above the natural frequency $f_0 = 1/(2\pi\sqrt{LC})$, the input voltage u_1 changes its polarity at instant 1 due to the turn-off of the high-side transistor before i_L becomes zero. Consequently, the system transits to state B where the sum $U_1 + U_2$ causes a high rate of current reduction [see Fig. 4(b)] according to the circular trajectory with the center point $[-(U_1 + U_2), 0]$. At instant 2, the current i_L becomes negative, the current in the rectifier diodes commutates, and u_2 again shows equal (i.e., negative) polarity as u_1 (state C); now $[-\Delta U, 0]$ is the new center of the trajectory valid until the lower power transistor turns off at instant 3 and the system passes over to state D (center $[+(U_1+U_2), 0]$) which completes a full cycle at instant 4.

For the practical realization of the series-resonant converter stage of the proposed system it is of importance that, in general, $\Delta U \ll U_1$ is valid; this is caused by the fact that the characteristic impedance $Z_0 = \sqrt{L/C}$ is defined by the small inductance L given to a significant extent by the transformer leakage. With this assumption, the system trajectory in good approximation shows the shape of Fig. 4(c), i.e., the current contribution of states B and D to i_2 can be neglected [$t_{1,2} \rightarrow 0$, Fig. 4(c)]. With this and using the conduction angle

$$\alpha = \frac{\pi}{\frac{f_S}{f_0}} \tag{1}$$

the equations

$$(\hat{u}_C + \Delta U)\cos(\pi - \alpha) = \hat{u}_C - \Delta U \tag{2}$$

and

$$Z_0 I_2 = (\hat{u}_C + \Delta U)\frac{1}{\alpha}\int_0^{\alpha} \sin(\omega t) d\omega t \tag{3}$$

can be written according to the geometric relations given by Fig. 4(c) and according to the fact that the average value of i_2 (i.e., the rectified inductor current i_L) in the stationary case is defined by the load current I_2. Evaluation of (3) and rearranging using (2) finally leads to

$$\Delta U = I_2 \cdot R_{\text{out}} \text{ with } R_{\text{out}} = Z_0 \frac{\frac{\alpha}{2}}{\tan^2\frac{\alpha}{2}} \tag{4}$$

and

$$\hat{u}_C = \frac{\alpha}{2} Z_0 I_2 = \frac{I_2}{4 f_S C}. \tag{5}$$

These equations state that, for a given switching frequency (fixed conduction interval α), the output voltage U_2 decreases proportional to the load current I_2, i.e., the converter shows a quasi-ohmic output impedance (current-independent output resistance R_{out}; see equivalent circuit given in Fig. 5).

Remark: This system behavior is very similar to the commutation voltage drop of line commutated converters where the commutation inductances finally cause a current-proportional output voltage reduction.

An exact calculation as given in [17] results in an output characteristic described by ellipses (see the thin curves in Fig. 5). However, as is indicated by the shaded area of Fig. 5, for the operating region being relevant for the proposed system ($\Delta U < 10\%$) the simplified calculation given here shows excellent accuracy. Fig. 6 demonstrates that the output impedance R_{out} is approximately linearly dependent on the switching frequency and $R_{\text{out}} \rightarrow 0$ for $f_S \rightarrow f_0$ is valid. Therefore, the desired stiff output characteristic suggests $f_S = f_0$. However, this would lead to a worse transient response (voltage overshoot) because

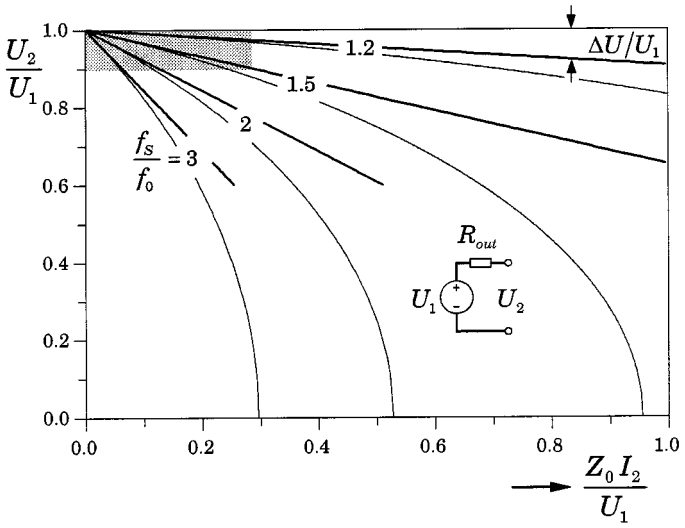


Fig. 5. Output characteristic of the series-resonant converter for fixed-frequency operation above the natural frequency.

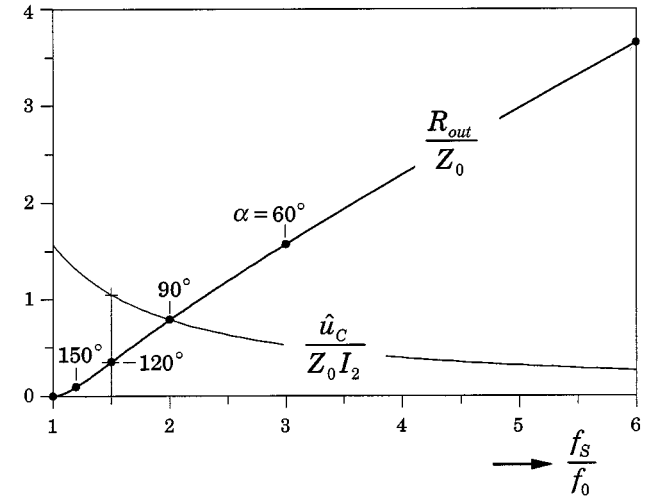


Fig. 6. Dependency of the output impedance $R_{\rm out}$ and of the capacitor peak voltage value $\hat{u}_C$ on the switching frequency.

$R_{\rm out}$ also acts as damping resistor for the resonant circuit given by the output inductance (not shown in the equivalent diagram of Fig. 5) and the output smoothing capacitor. Furthermore, it has to be taken into account that the turn-off of the power transistors has to be performed at $i_L > 0$; only in this case there exists a remaining current which charges the drain-source capacitance of the transistors in order to get zero-voltage turn-on. For a practical realization the resonant network typically is dimensioned to achieve $\alpha \approx 120°$ (i.e., $f_S = 1.5 f_0$).

B. Practical Design and Realization

Concerning the design of the multicell converter with the key specifications as given at the beginning of Section II (rated power 2 kW in a four-cell arrangement) the specifications of the dc–dc isolation stage are defined by the following:

dc input voltage $U_1 = 100$ V (80–120 V);
dc output voltage $U_2 \approx U_1$ (1:1 transfer ratio);

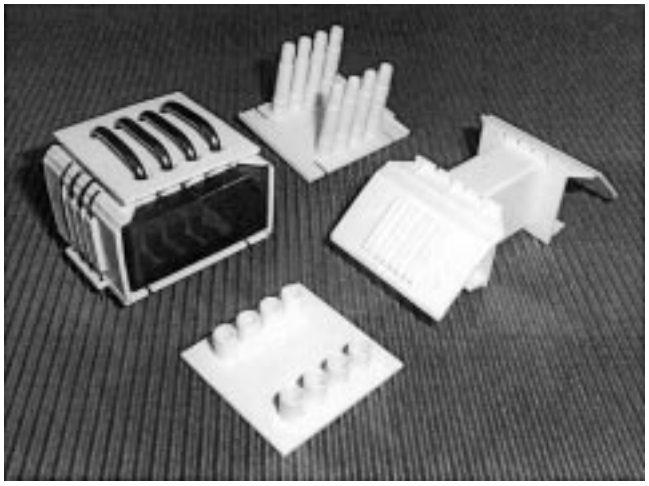


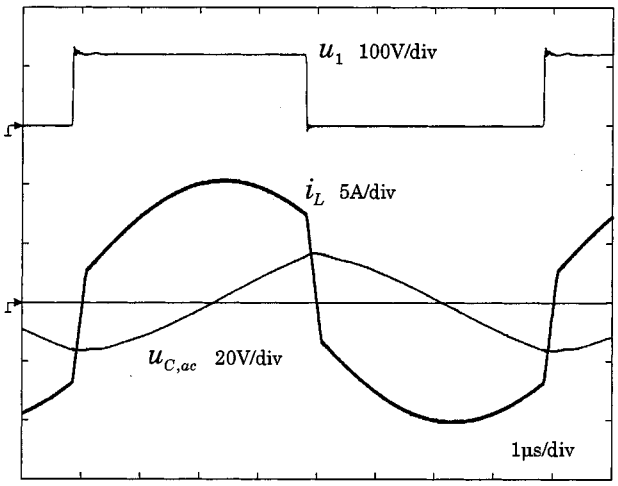
Fig. 7. Transformer of the resonant 500-W dc–dc converter using "bow winding" technique (shown here for $N_1 = 4$) for direct PCB mounting and components of the coil former.

rated power $P_N = 500$ W;
switching frequency $f_S \approx 100$–125 kHz.

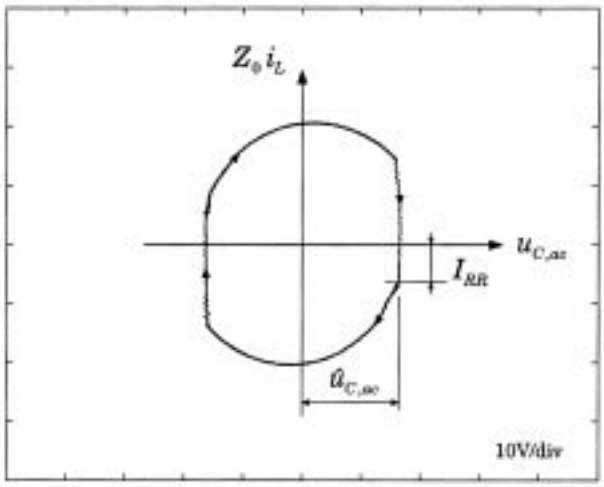
For the two power MOSFETs the SiliconMAX devices PSMN035-150P (TO220 type package, 150 V, 35 mΩ) have been chosen. The gate drive is realized using an IR2113 driver circuit with additional turn-off speedup using two p-n-p transistors BC327 to enhance the discharge of the MOSFET gate. The center tapped rectifier on the secondary side of the transformer is equipped with an MUR1640 (2×8 A, 400 V) diode.

The power transformer is, as already mentioned at the beginning of Section III, realized by application of the "bow winding principle," i.e., the primary winding is formed by $N_1 = 5$ copper bows ($\varnothing$2.5 mm) on the selected E42/21/20 ferrite core (material: N87). The secondary windings ($N_2 = 2 \times 10$ turns to get a 1:1 voltage transfer ratio of the converter, $\varnothing$1 mm) are implemented using conventional winding techniques. A coil former of specific shape (see Fig. 7) is applied to get a compact transformer design and to guarantee the required creepage and clearance distances. The dimensioning data given before cause a peak flux density of $\hat{B} \approx 100$ mT resulting in core losses of $P_{Fe} \leq 3$ W at ($U_1 = 120$ V, $f_S = 125$ kHz, $T = 100$ °C) as specified by the data sheet. Although the proposed winding technique does not show very tight coupling, the stray inductance of the transformer is too low and a small additional choke (five turns of litz wire on a single ETD29 leg (half core set)) has to be used for adjusting the natural frequency of the resonant circuit to $f_0 \approx 80$ kHz. With the applied resonance capacitors ($2 \times 5 \times 0.1$ μF polyester-foil-type components in parallel, $C = 1$ μF) for $f_S = 125$ kHz this results in

$$
\begin{aligned}
L &\approx 4\,\mu\text{H} \\
Z_0 &= \sqrt{\frac{L}{C}} = 2\,\Omega \\
\frac{f_S}{f_0} &\approx 1.5 \\
\alpha &\approx 120° \\
R_{\rm out} &\approx 0.7\,\Omega \\
\hat{u}_C &\approx 16\text{ V at } I_2' = 4\text{ A}
\end{aligned}
$$



(a)



(b)

Fig. 8. (a) Measured voltage and current wave shapes and (b) measured system trajectory of the laboratory prototype of the series-resonant dc–dc converter; parameters:$U_1 = 120$ V, $f_S = 125$ kHz, and $P \approx 440$ W.

using the equations of Section III. Concerning $R_{\rm out}$, it has to be noted that $R_{\rm out}$ specifies the output impedance related to the primary side of the transformer; this value has to be multiplied by $(N_2/N_1)^2 = (10/5)^2 = 4$ for characterizing the output (load-side) behavior of the converter.

C. Laboratory Prototype System—Measurements

The measurements (see Fig. 8) taken from the laboratory model show a close correspondence to the theoretical wave shapes as given in Fig. 4 with the exception that the real system shows a significant reverse-recovery current $I_{\rm RR} \approx 3.5$ A of the rectifier diodes; this matches also with the datasheet specifications of MUR1640 for $di/dt \approx 40$ A/μs. The loss measurements demonstrate an efficiency of 96.3% at rated power (500 W) for 110-kHz switching frequency (Fig. 9). The partial load region is characterized by efficiency values up to 97%. It has to be noted that the rectifier diodes contribute to about up to 50% of the total losses. This suggests the application of synchronous rectification circuit extensions as will be

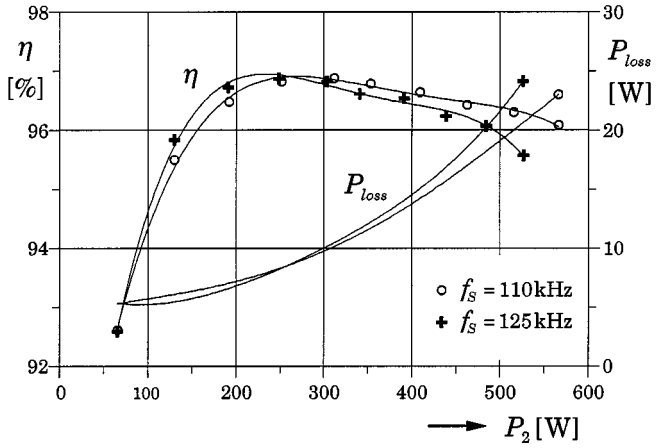


Fig. 9. Measured losses and efficiency of the prototype dc–dc isolation stage; parameters: $U_1 = 120$ V.

proposed in Section V. Furthermore, the switching losses could be optimized by implementation of a load-dependent interlock delay time of the driver stage or, alternatively, by application of a driver stage with inherent $u_{DS} = 0$ turn-on capability (according to the dual-thyristor principle as described in [17]) to achieve true zero-voltage switching within the entire load region.

IV. Multicell DC–AC Converter

For the description of the dc–ac converter for generating the 230-$V_{\rm rms}$ ac output of the system, one should refer to a large extent to the analyses of the multi-cell class-D switch-mode amplifier presented in [18]. It has to be pointed out that the essential benefit of the multicell topology is that, if the N individual switching cells are operated in an interleaved PWM mode, the output current ripple is reduced by a factor of N^2. By application of a second-order *LC* output filter, the output voltage ripple across the filtering capacitor is reduced by N^3 according to [18, eqs. (5) and (6)], i.e., for $N = 4$ the ripple is reduced by a factor of 64 as compared to a single-cell topology, e.g., given in Fig. 1(b). This makes it possible to operate the system at a comparatively low PWM switching frequency. For the realized prototype system, a single-cell switching frequency of $f_S = 1$ kHz has been chosen. Due to the 1:1 voltage transfer ratio of the dc–dc converter the power stages of the dc–ac converter can be equipped with the same type of power MOSFETs as used for the isolation stage ($4 \times 4 = 16$ pieces of PSMN035-150P 150-V/35-mΩ devices).

A. PWM Pattern Generation

The pattern generation for the interleaved PWM is performed by a circuit showing remarkably low effort (see [18, Fig. 7]). First, a simple CD4047 IC oscillator generates the basic clock ($4f_S$) of the modulator. Subsequently, a "tree" of six toggle flip-flops (three pieces of CD4013) forms four interleaved rectangular signals feeding the inputs of four analog integrator stages realized by a single TL084 operational amplifier IC. At the integrator outputs four phase-shifted triangular signals

appear which define the carrier signals for the total of eight comparators (two pieces of LM339). These devices act as a PWM stage comparing the carrier signals with the reference signals $\pm u_{\rm ref}$ (i.e., in this case, a 50-Hz sinusoidal signal) of the output voltage. The LM339 ICs directly drive eight simple low-cost optocouplers (SFH606) which are used to provide the required isolation between the PWM generator and the (floating) driver stages of the switching cells. Interlock timing and gate drive of the power MOSFETs of a half-bridge arrangement is performed using eight standard integrated driver ICs (IR2111). The auxiliary supply of these devices is provided by small 0.5-W standard dc–dc converters. The whole PWM pattern generation, control, and gate drive of the dc–ac converter fits on a single 160×100-mm PCB using standard (non-SMD) components. The power consumption of the total board (including driver stages) has been measured to be $\leq$ 1.8 W.

B. Output Filter—Voltage Control

The presented prototype system has been designed for stand-alone applications only and not for feeding energy to the public mains. For the latter application, the voltage is defined by the mains and the converter would have to be equipped with an output current control to ensure a voltage-proportional mains current of corresponding amplitude. For stand-alone applications, the output voltage u_O is defined by the PWM control of the converter. In the simplest case—as implemented for the realized laboratory setup—an open-loop control can be applied. However, with this, the damping of the *LC* output filter has to be performed exclusively by the impedance of the load. If a pure ohmic load characteristic $Z_{\rm out} = R_{\rm out}$ is guaranteed, a sufficient damping is achieved if $Z_0 \geq R_{\rm out}$ is valid for the characteristic impedance $Z_0 = \sqrt{L/C}$ of the *LC* filter. For $R_{\rm out} = 26\,\Omega$ (i.e., output power 2000 W at $U_{\rm out} = 230\ {\rm V_{rms}}$) filter components of $L \approx 2$ mH and $C = 3\ \mu$F have been selected resulting in a cutoff frequency of $f_0 \approx 2$ kHz and a characteristic impedance of $Z_0 \approx 26\,\Omega$. However, in the case of no-load or light-load operation or for reactive load, this load-based damping fails and an additional damping branch (e.g., a $R_D C_D$-series snubber arranged in parallel to the filter capacitor C, typical values:$R_D \approx Z_0$, $C_D \approx 3C$) would be required leading to additional losses appearing in the damping branch (i.e., in R_D). The drawback of the reduced efficiency of this solution can be avoided if an "active" damping of the *LC* output filter is performed. Implementing a negative feedback of the filter capacitor current to the reference voltage input of the PWM stage (feedback coefficient R_{FB}) gives the desired shift of the poles of the *LC* filter to the left side of the s plane (see [18]). Choosing, e.g., $R_{FB} = Z_0/\sqrt{2}$ results in a Butterworth response of the system.

However, as indicated by [18, Fig. 10] even for active filter damping the output voltage quality is low if nonlinear loads (e.g., diode-bridge rectifiers) are supplied. Analysis of the low-frequency harmonics give a total harmonic distortion (THD) $\approx$7% of u_O for a diode-bridge rectifier load according to the following parameters: $L_{\rm IN} = 1$ mH, $C_{\rm DC} = 2$ mF, $I_{\rm DC} = 5$ A; $I_{N,{\rm RMS}} = 10.2$ A, ($P = 1550$ W, $S = 2340$ VA, and $\lambda = 0.66$). This behavior is originated by the output impedance of the

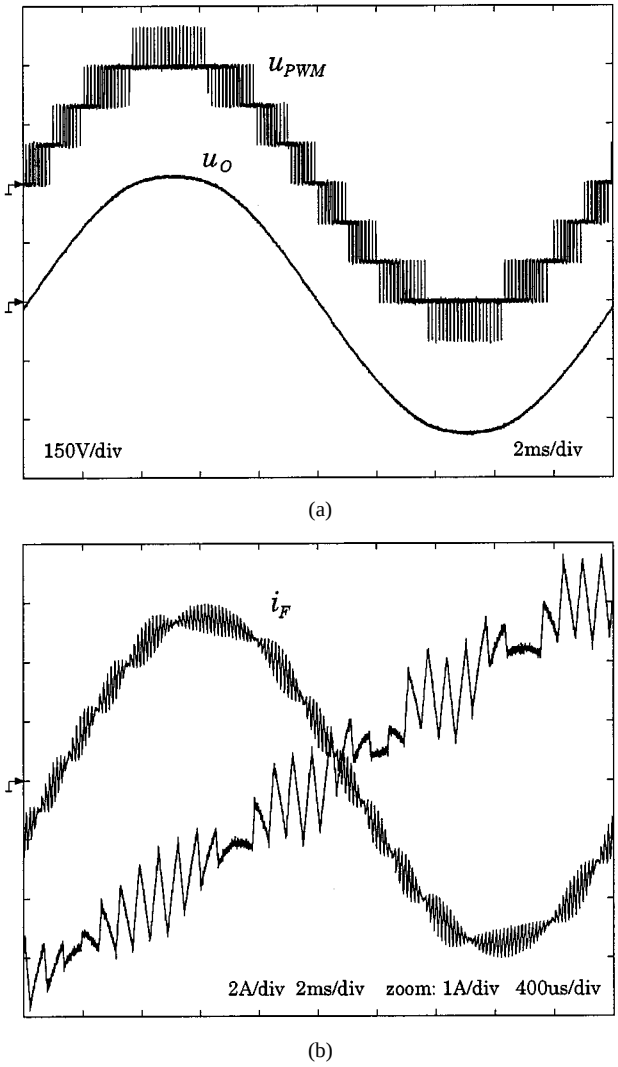


Fig. 10. (a) AC output voltage (u_{PWM}: before filtering; u_O: after *LC* output filter having a cutoff frequency of $\approx$ 2 kHz) and (b) output filter inductor current i_F of the dc–ac converter laboratory prototype; parameter: $f_S = 1$ kHz.

LC filter which can be lowered very much using a closed-loop control of the total output voltage. Using a simple proportional-plus-integral (PI)-type controller reduces the output harmonics for the load mentioned before to a THD of $\leq$2%. A detailed description of the dimensioning of the controller is given in [18, Sec. IV] and shall be omitted here for the sake of brevity. More sophisticated results would be achievable if a multiloop control (e.g., current control with superimposed output voltage control and feed-forward of the load current) is applied.

C. Laboratory Prototype System—Measurements

The measurement results of the prototype system illustrate the multilevel voltage generation of this multicell topology [see converter output voltage $u_{\rm PWM}$ in Fig. 10(a)]. The ripple of the current i_F through the output filter inductor shows "nodes" being typical for a multilevel approach [Fig. 10(b)]. Across the filter capacitor there appears the very smooth ac output voltage u_O of the system. As indicated by the Fourier analysis of the unfiltered output voltage $u_{\rm PWM}$ (Fig. 11), significant harmonic

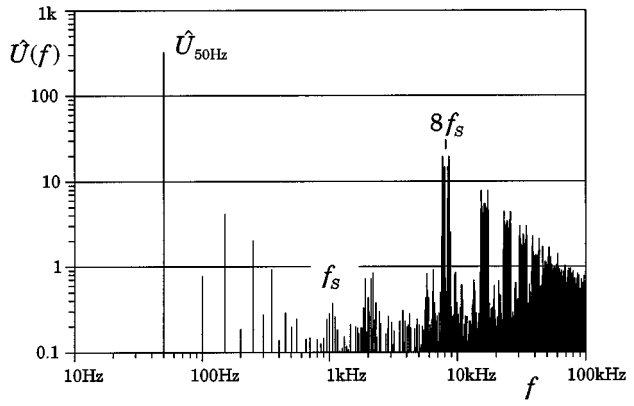


Fig. 11. Frequency components of the *unfiltered* converter output voltage u_{PWM}. The harmonics in the frequency range 100–700 Hz are due to a nonideal behavior of the duty-cycle limiting stage which is required to guarantee the operation of the charge pump of the IR2111 driver.

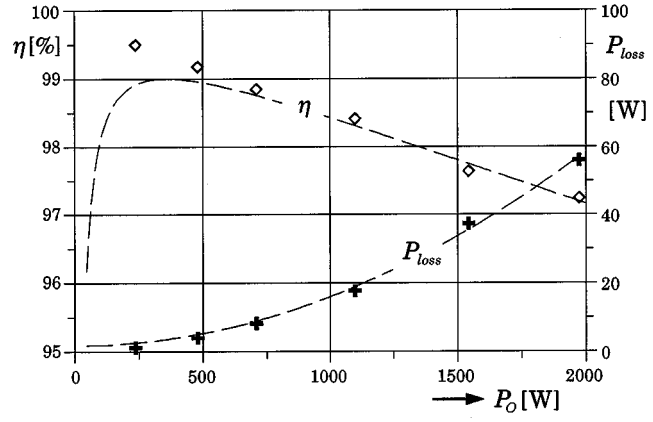


Fig. 12. Efficiency and losses of the dc–ac converter. The characteristics shown by the dashed curves give an approximation based on an ideal 230-V voltage source with 0.75-Ω output resistance and 1.8-W permanent no-load losses. Furthermore, the diagram demonstrates the sensitivity to measurement errors, especially for very-high-efficiency values because the dashed curve in any case defines an upper limit for the efficiency.

components exist only in the vicinity of multiples of $2Nf_S$, i.e., for $f_S = 1$ kHz, here, in the vicinity of 8 kHz, 16 kHz, etc., due to the cancellation of all lower frequency components according to the interleaved PWM mode.

As indicated by Fig. 12, the dc–ac converter shows the expected excellent efficiency due to the low $R_{DS,\mathrm{on}}$ of the power transistors in connection with the almost negligible switching losses. However, it has to be noted that the accurate measurement of the losses of ultraefficient converters requires very precise testing equipment; even very low measurement errors show a serious impact on the resulting efficiency/loss characteristic of the tested converter. In particular, for the case where prototypes of different systems are tested using different measurement equipment, the measurements and the comparison of the results should be performed very carefully.

V. Conclusions and Future Developments

With the proposed multicell multilevel converter topology, energy conversion to the mains voltage level (230 V_{RMS} is possible using exclusively MOSFETs with comparatively low-rated voltage. These devices are characterized by a very low on-state voltage drop which results in low conduction losses. Due to the interleaved switching of the individual cells, the output voltage ripple of the total system is small and, therefore, good mains behavior (i.e., low mains current harmonics) can be achieved although the PWM of a single cell is based on a low switching frequency (causing only low switching losses). Consequently, the converter shows very high efficiency. Because the voltage control of the system is performed by PWM of the dc–ac converter, the dc–dc converter being required for feeding the floating dc–ac stages can be realized by application of an uncontrolled fixed-frequency series-resonant topology. Equal MOSFET devices can be applied for the dc–dc stage and for the dc–ac converter because of similar voltage levels of the design used. The high quantity of required power semiconductor devices (e.g., 24 transistors plus 12 half-bridge driver circuits for the designed 2-kW prototype) might be seen as a drawback of the proposed topology. However, on the other hand, this does allow the application of low-cost standard power semiconductors; the low total losses distributed to a high number of power transistors (i.e., the more uniform heat distribution) significantly simplifies the system cooling. To demonstrate this circumstance, it should be mentioned that the prototype dc–ac converter can be operated at 50% of the rated power (i.e., at 1 kW) *without any heat sink.*

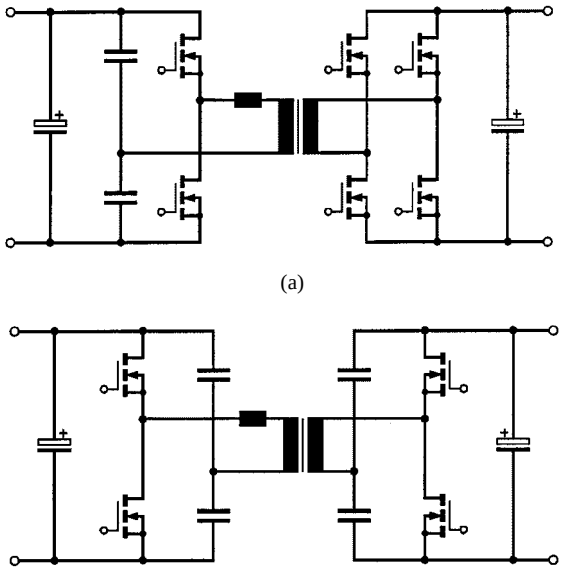


Fig. 13. Extension of the resonance-mode dc–dc converter to (a) synchronous rectification and (b) to bidirectional operation.

As mentioned in Section III, concerning future developments it would be of interest to apply synchronous rectification to the dc–dc isolation stages because the on-state losses of the diodes contribute considerably to the total system losses. In this case, however, it would be preferable to change to a full-bridge circuit as shown in Fig. 13(a) due to the improved efficiency caused by the basic physical characteristics of the majority of carrier-based semiconductors (in theory, $R_{DS,\mathrm{on}} \propto U_{DS,\mathrm{max}}^{2.6}$) and to allow the

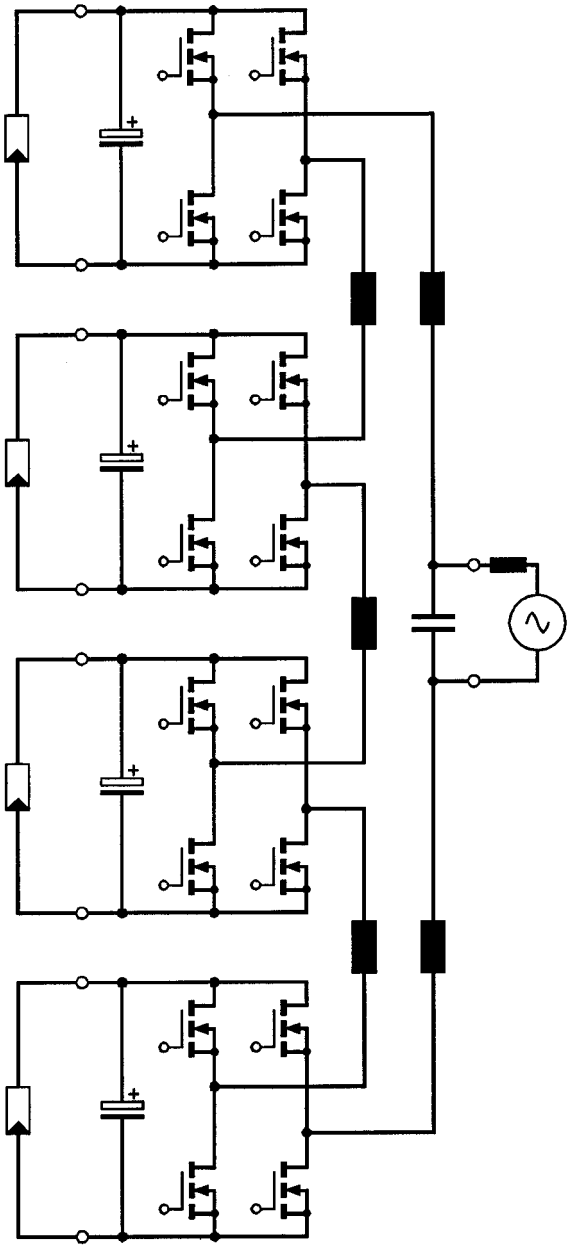


Fig. 14. Application of the multicell topology to nonisolated solar converter systems.

application of transistors of the same type for the input and output sections of the converter. In principle, the converter of Fig. 13(a) also permits a bidirectional power flow. This operation mode would be of interest if the system is utilized for supercapacitor or battery-based systems (e.g., uninterruptable power supplies, power flow equalizer systems, etc.) to recharge the energy storage device on the dc input. It should be mentioned that the dc–ac converter using the proposed multicell arrangement itself intrinsically permits a full four-quadrant operation. (This is of special importance also for reactive power generation if the system is used for stand-alone applications not being connected to the mains.) However, the converter of Fig. 13(a) does provide a dc current path on the secondary which might result in saturation of the core. This can be avoided by application of a secondary-side blocking capacitor, or, alternatively, by splitting up the resonance capacitor to both transformer windings as shown in Fig. 13(b).

Finally, the multicell converter topology should also be proposed for nonisolated solar power systems as shown in principle in Fig. 14. Despite the fact that the solar panels show significant common-mode voltages (which have to be lowered by current-compensated input chokes) and that a relatively complex control is required to achieve low ac harmonics also for different dc input voltages with maximum power point (MPP) tracking, this topology could gain attention due to its ultrahigh efficiency. This multicell structure might also be of interest for the realization of "distributed" power photovoltaic converters.

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