Hybrid Multilevel Converters: Unified Analysis and Design Considerations

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***Abstract*—The concept of hybrid multilevel converters has been generalized for different arrangements of direct-current voltage levels, modulation strategies, topologies of series-connected cells, and/or semiconductor technologies to optimize the power processing of the overall system. Therefore, a given number of levels can be synthesized by several multilevel configurations, significantly increasing flexibility and complexity in the design of hybrid multilevel converters. However, a generalized design methodology to define the main parameters of these topologies for distinct design criteria has not yet been presented. To overcome this lack, this paper presents a comparative analysis among various hybrid multilevel topologies, and it proposes some design considerations for distinct applications. Consequently, this paper constitutes a useful basis for defining an adequate hybrid arrangement for any application.**

***Index Terms*—High-power applications, multilevel systems.**

NOMENCLATURE

f_1	Switching frequency of the lowest power cell.
K_n	Coefficient defined in (17).
m	Number of levels of the phase-to-neutral output voltage.
m_a	Amplitude modulation index.
m_j	Number of levels synthesized by the jth cell $(j = 1, 2, \ldots, n)$.
$m_{\min}$	Minimum number of levels for nominal amplitude modulation index.
n	Number of series-connected cells.
$r_j(t)$	Reference signal of the jth cell.
S	Number of switching devices per phase.
$V_{\text{fund},j}$	Fundamental voltage synthesized by the jth cell.
$v_a(t)$	Phase "a"-to-neutral output voltage.
$v_{a,j}(t)$	Output voltage of the jth cell in phase a.
$V_{\text{dc},j}$	Total dc-bus voltage of the jth cell.
V_j	Normalized voltage step synthesized by the jth cell.
$V_{\max,j}$	Maximum normalized voltage step of the jth cell.
$\Delta V_{\text{dc},j}$	Voltage step between two adjacent levels of the jth cell.
σ_j	Maximum normalized instantaneous voltage synthesized by j first cells, corresponding to the sum of the dc bus voltages of the j first cells.
$\Psi_{n,i}$	ith comparison level used at the low-frequency modulation strategy of the nth cell.

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I. INTRODUCTION

IN RECENT years, asymmetrical multilevel inverters have received increasing attention because it is possible to synthesize voltage waveforms with reduced harmonic content, even using a few series-connected cells. This advantage is achieved by using distinct voltage levels in different cells, which can create more levels in the output voltage and minimize its total harmonic distortion (THD) without increasing the number of switching devices and isolated sources [1]–[17]. As a result, it is possible to reduce or even to eliminate output filters. On the other hand, the use of different voltage levels leads to a smaller modularity in comparison to symmetrical multilevel inverters.

Conventional pulsewidth-modulation (PWM) techniques could be used to move the harmonics to higher frequencies. However, conventional PWM strategies are not suitable for asymmetrical multilevel inverters because the switching devices of the higher voltage cells would have to operate at high frequency during some time intervals [8], [9]. Consequently, a hybrid modulation strategy was proposed in [10] and [11], so that higher power cells operate at low frequency and only the lowest power cell operates with high-frequency PWM. With this strategy, it is possible to use slow semiconductor devices in the higher voltage cells and also to employ fast semiconductor devices in those cells operating with reduced voltage levels, drawing from distinct semiconductors technologies. Therefore, hybrid multilevel inverters can be defined as those systems composed of several series-connected cells that present different dc voltage levels, modulation strategies, topologies, and/or semiconductor technologies operating in synergism.

Based on these principles, the concept of hybrid multilevel converters can be generalized for different arrangements of dc voltage levels and distinct topologies of multilevel cells, increasing significantly the flexibility and the complexity of their design. Nevertheless, a detailed unified approach for hybrid multilevel converters, including both a comparative analysis among several configurations and a generalized design methodology to define the main parameters of these topologies, has not yet been presented.

To fill this gap, this paper presents a comparative analysis among several hybrid multilevel converters, and it proposes some design considerations to minimize the number of

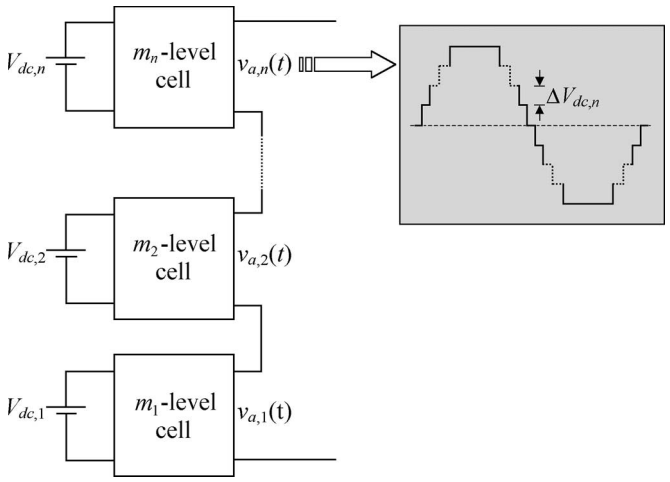


Fig. 1. Generalized structure of one phase of a voltage-source multilevel inverter.

switching devices, to reduce the circulating energy among the series-connected cells, and to take into account the topology of the input rectifier stage and the voltage ratings of the switching devices, so that it is possible to define an adequate topology for any application.

This paper is organized as follows. Section II describes the generalized structure of a hybrid multilevel converter, including some restrictions that should be respected to synthesize low-THD output voltages. Section III proposes several design considerations for hybrid multilevel converters, and it also presents an important comparative analysis among distinct topologies. Section IV includes a design example, and Section V shows some experimental results to demonstrate the functionality of hybrid multilevel converters.

II. Hybrid Multilevel Converters

Fig. 1 shows the generalized structure of one phase of a voltage-source multilevel inverter with n multilevel dc–ac cells connected in series. A phase-to-neutral voltage waveform is obtained by adding up the output voltages of each cell, e.g.,

$$v_a(t) = v_{a,1}(t) + v_{a,2}(t) + \cdots + v_{a,n}(t). \tag{1}$$

It is considered that the output voltage of the jth cell presents m_j equally spaced levels, where the voltage step between two adjacent levels is $\Delta V_{\mathrm{dc},j}$, as shown in Fig. 1. Several topologies of single-phase dc–ac cells, such as those presented in Fig. 2, can be connected in series to obtain multilevel waveforms [6], [7]. Full-bridge cells are usually employed because they use a smaller dc bus voltage level, and they present a smaller number of components than half-bridge cells with the same number of levels, as shown in Fig. 2(b) and (c) for three-level cells. On the other hand, full-bridge cells cannot synthesize voltage waveforms with an even number of levels. Although each configuration has its advantages and disadvantages, the unified analysis presented hereinafter does not depend on the arrangement adopted to obtain a given number of levels.

When all series-connected multilevel cells synthesize waveforms with the same voltage step (voltage amplitude between two adjacent levels), it can be demonstrated that the number of phase-to-neutral voltage levels m obtained with the multilevel inverter shown in Fig. 1 is

$$m = 1 + \sum_{j=1}^{n} (m_j - 1). \tag{2}$$

Thus, it would be necessary to add more cells in series and/or increase the number of levels synthesized by some cells to obtain output voltage waveforms with a larger number of levels. On the other hand, the number of levels can be increased, without increasing the number of devices, when the waveform generated by at least one cell has a voltage step that differs from those obtained by other cells. In this case, the inverter shown in Fig. 1 can be called an asymmetrical multilevel inverter [2]–[6].

For this unified analysis, the series-connected cells are arranged in increasing order, so that the nth cell presents the highest voltage step. Then,

$$\Delta V_{\mathrm{dc},1} \leq \Delta V_{\mathrm{dc},2} \leq \cdots \leq \Delta V_{\mathrm{dc},n-1} \leq \Delta V_{\mathrm{dc},n}. \tag{3}$$

Moreover, the lowest voltage step $\Delta V_{\mathrm{dc},1}$, which also corresponds to the voltage step of the output multilevel waveforms, is defined as the voltage base value for the per unit (p.u.) notation. Consequently, the normalized voltage step synthesized by the jth cell can be expressed as

$$V_j = \frac{\Delta V_{\mathrm{dc},j}}{\Delta V_{\mathrm{dc},1}}, \qquad j = 1, 2, \ldots, n. \tag{4}$$

The normalized voltage steps of all cells must be natural numbers (i.e., $V_j \in \mathbb{N}$) and must also satisfy the following condition to generate output waveforms with equally spaced voltage levels [4]:

$$V_j \leq 1 + \sum_{k=1}^{j-1} (m_k - 1) V_k \tag{5}$$

where m_k is the number of levels and V_k is the normalized step synthesized by the kth cell.

This restriction can be rewritten as

$$V_j \leq 1 + 2\sigma_{j-1} \tag{6}$$

where σ_{j-1} is the maximum normalized voltage synthesized by $j-1$ first cells, which is given by

$$\sigma_{j-1} = \sum_{k=1}^{j-1} \frac{(m_k - 1) V_k}{2}. \tag{7}$$

Considering that (5) is satisfied, an asymmetrical multilevel inverter can generate phase-to-neutral voltage waveforms with the following normalized voltage levels:

$$v_a(t) = \{-\sigma_n, -(\sigma_n - 1), -(\sigma_n - 2), \ldots, (\sigma_n - 2), (\sigma_n - 1), \sigma_n\}. \tag{8}$$

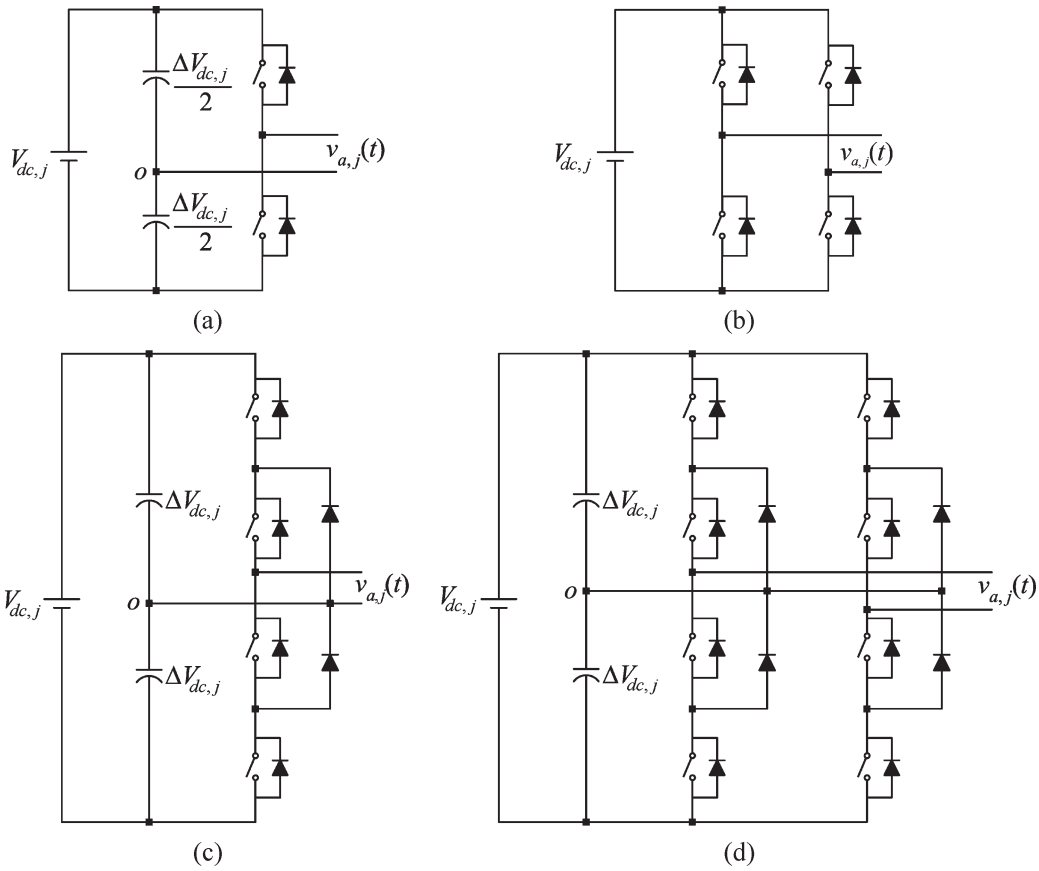


Fig. 2. DC–AC cells. (a) Two-level cell. (b) Full-bridge three-level cell (H-bridge). (c) Half-bridge three-level cell. (d) Full-bridge five-level cell.

As this set is composed of elements varying in arithmetic progression, it can be demonstrated that the number of phase-voltage levels synthesized by an asymmetrical inverter is

$$m = 1 + 2\sigma_n \tag{9}$$

or using (7),

$$m = 1 + \sum_{j=1}^{n} (m_j - 1)V_j. \tag{10}$$

From (2) and (10), it is possible to verify that asymmetrical multilevel inverters can generate a larger number of levels with the same number of series-connected cells. In addition, the same number of levels can usually be obtained from different combinations of voltage steps, numbers of series-connected cells, and/or topologies since σ_n is the same.

A. Generalized Modulation Strategy

A hybrid modulation strategy for asymmetrical multilevel inverters was presented in [10] for three-level series-connected cells, in which only the lowest power cell operates with PWM. Other cells, which operate with higher voltage levels and could employ high-voltage semiconductor devices, operate at low frequency. This strategy can be generalized for multilevel cells, as shown in the simplified block diagram of Fig. 3(a).

One can see that the reference signal of the hybrid multilevel inverter is the reference signal of the nth cell. This signal is compared to a given number of constant levels, which depend on the number of levels synthesized by this cell, as presented in Fig. 3(b) and (c). For a cell that generates an odd or even number of levels, the ith comparison level of the nth cell $(\Psi_{n,i})$ can be given as [16]

$$\Psi_{n,i} = \sigma_{n-1} + (i-1)V_n, \quad i = 1, \ldots, (m_n - 1)/2 \text{ for odd } m_n \tag{11}$$

$$\Psi_{n,i} = \sigma_{n-1} + (2i-1)\frac{V_n}{2}, \quad i = 1, \ldots, (m_n - 2)/2 \text{ for even } m_n. \tag{12}$$

After determining the desired output voltages of the higher power cells, the reference signal of the jth cell is obtained by subtracting the output voltage of the $j+1$ cell from its respective reference signal. This reference, which corresponds to the voltage that higher power cells could not synthesize, is also compared to several constant levels. Finally, the reference signal of the lowest power cell is compared to high-frequency triangle signals with amplitude V_1 and frequency f_1, resulting in a high-frequency voltage [18].

However, to synthesize voltage waveforms modulated at high frequency among all adjacent voltage steps, the normalized voltage steps of all cells must satisfy the following condition [4], [14]:

$$V_j \leq \sum_{k=1}^{j-1} (m_{k-1})V_k. \tag{13}$$

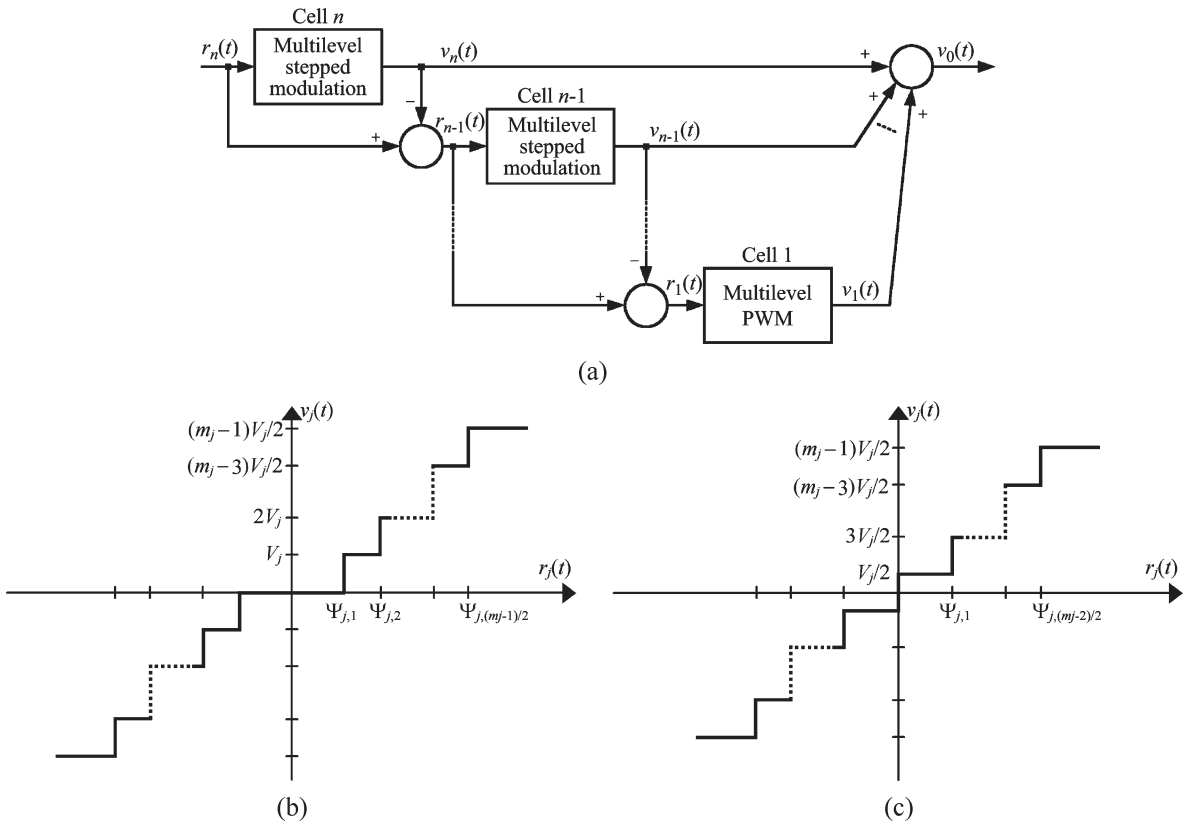


Fig. 3. Generalized hybrid modulation strategy. (a) Block diagram. (b) Stepped modulation for multilevel cells with an odd number of levels. (c) Stepped modulation for multilevel cells with an even number of levels.

TABLE I
LIMITING VALUES OF V_j TO SYNTHESIZE VOLTAGE WAVEFORMS MODULATED AT HIGH FREQUENCY

Cells	V_j (p.u.)
2-level	$1, 1, 2, ..., 1\times2^{n-2}$
3-level	$1, 2, 6, ..., 2\times3^{n-2}$
4-level	$1, 3, 12, .., 3\times4^{n-2}$
5-level	$1, 4, 20, ..., 4\times5^{n-2}$
⋮	⋮
m_j-level	$1, (m_j-1), (m_j-1)m_j, ..., (m_j-1)m_j^{n-2}$

By respecting this restriction, the output voltage harmonics will be concentrated around the frequency multiples of the switching frequency of the lowest power cell.

Using (7), this restriction can be rewritten in another form, i.e.,

$$V_j \leq 2\sigma_{j-1}. \tag{14}$$

As an example, Table I lists the limiting values of V_j, which are computed from (13), to generate output voltages modulated at high frequency among all adjacent steps, when all series-connected cells are able to synthesize the same number of levels.

B. Example of a Hybrid Multilevel Inverter

To exemplify the generalized operating principles of hybrid multilevel converters, Fig. 4 presents a hybrid multilevel inverter with two-, three- and five-level cells connected in series.

Fig. 5 presents the reference and output voltage waveforms of the three cells that compose the hybrid inverter shown in Fig. 4 for a unitary amplitude modulation index m_a. The first cell synthesizes two levels with 1-p.u. voltage step, the second cell generates three levels, also with 1-p.u. voltage step, and the third cell synthesizes five levels with 3-p.u. voltage steps. The switching devices of the two-level cell operate at high frequency, while the switches that compose the five-level cell operate at fundamental frequency. As V_1, V_2, and V_3 satisfy (13), the phase-voltage waveform with 16 levels is modulated at high frequency among any adjacent levels, as illustrated in Fig. 5(d).

This example demonstrates the wide variety of arrangements that can be adopted to obtain a given number of levels. Thus, it is essential to develop a design methodology to define the main parameters of a hybrid inverter, such as the number of series-connected cells, dc voltage levels, and topologies used in each cell.

III. DESIGN CONSIDERATIONS AND COMPARATIVE ANALYSIS

This section presents a detailed comparative analysis among distinct hybrid multilevel converters, and it also includes a design methodology to minimize the number of switching devices. Other design considerations are proposed to reduce the circulating energy among the series-connected cells and to take into account the topologies used to obtain the dc voltage sources and the voltage ratings of semiconductor devices.

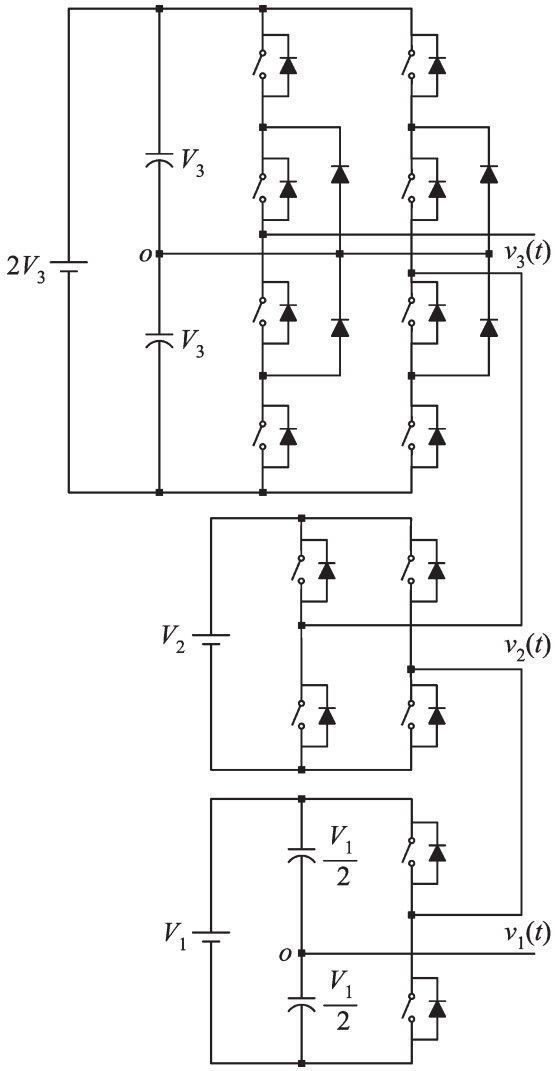


Fig. 4. Example of a hybrid multilevel converter with distinct series-connected cells.

A. Minimum Number of Switching Devices

According to (10), it is possible to maximize the number of levels synthesized by a hybrid multilevel converter without including other power devices, by using the maximum allowable values for V_j (13). From Table I, it is possible to notice that the limiting values of V_j vary according to a geometric progression with a ratio equal to m_j when all cells generate the same number of levels. For this case, the maximum number of phase-voltage levels can be given as

$$m = 1 + (m_j - 1)m_j^{n-1}. \tag{15}$$

Assuming that all power devices used in a given cell are subjected to the same voltage levels and all cells synthesize the same number of levels, the number of switching devices per phase S is

$$S = 2(m_j - 1)n. \tag{16}$$

Fig. 6 shows the maximum number of levels synthesized by distinct hybrid multilevel inverters, using only two-, three-, or five-level cells, for different numbers of switching devices per phase. It is possible to observe that a larger number of levels can be synthesized with a given number of switching devices by using only two-level cells. Therefore, one can affirm that this arrangement generates a given number of levels with the minimum number of switches. Any other configuration, using equal or distinct multilevel cells, employs a number of switches that is larger than that used with only two-level cells.

After defining the number of levels that the inverter should generate, Fig. 6 indicates the minimum number of switching devices per phase and, therefore, the number of two-level cells that should be connected in series to obtain this number of levels. Moreover, the normalized voltage steps synthesized by each cell can be obtained from Table I. Due to the fact that the two first cells synthesize voltage waveforms with 1-p.u. voltage steps, it is possible to replace these cells by a single three-level cell. Thus, the number of isolated sources can be reduced without affecting the number of levels for a given number of switching devices.

B. Reduction of the Circulating Energy

Depending on the voltage steps synthesized by series-connected cells, there can be a circulating energy among themselves [11], [15]. As this reactive energy increases the losses of the system, it is necessary to eliminate or to minimize this circulating energy.

Fig. 7 presents the fundamental voltages generated by four two-level cells, using $V_1 = V_2 = 1$ p.u., $V_3 = 2$ p.u., and $V_4 = 4$ p.u., by varying the output voltage amplitude $(0 \leq m_a \leq 1)$. With only eight switches per phase, this configuration is able to obtain a nine-level phase-voltage waveform modulated at high frequency among all adjacent steps. However, the fourth cell synthesizes a fundamental component that is larger than the fundamental output voltage for low m_a values, resulting in an excessive power processing that should be regenerated to the input source by other cells.

As the nth cell processes the highest power levels, the power processed by this cell should not be larger than the amount drawn by load, so that the circulating energy among the cells is reduced without significantly affecting the output number of levels for a given number of switches. Thus, it is necessary to verify the maximum voltage step V_n that the highest power cell can synthesize while satisfying this condition [15]. From (14), one can see that

$$V_n = K_n \sigma_{n-1}, \qquad K_n \leq 2. \tag{17}$$

Fig. 8 presents the fundamental voltage synthesized by the highest power cell by using distinct values of K_n and, therefore, of V_n, and also different topologies for this cell. Due to the fact that the output voltage of a two-level cell is equal to $V_n/2$ when the reference signal is positive and is equal to $-V_n/2$ when the reference is negative, its fundamental voltage remains constant for any amplitude modulation index, as presented in Fig. 8(a). Then, when a two-level cell is used in the highest power cell, it synthesizes a fundamental voltage that is greater than the output fundamental voltage for a wide m_a range,

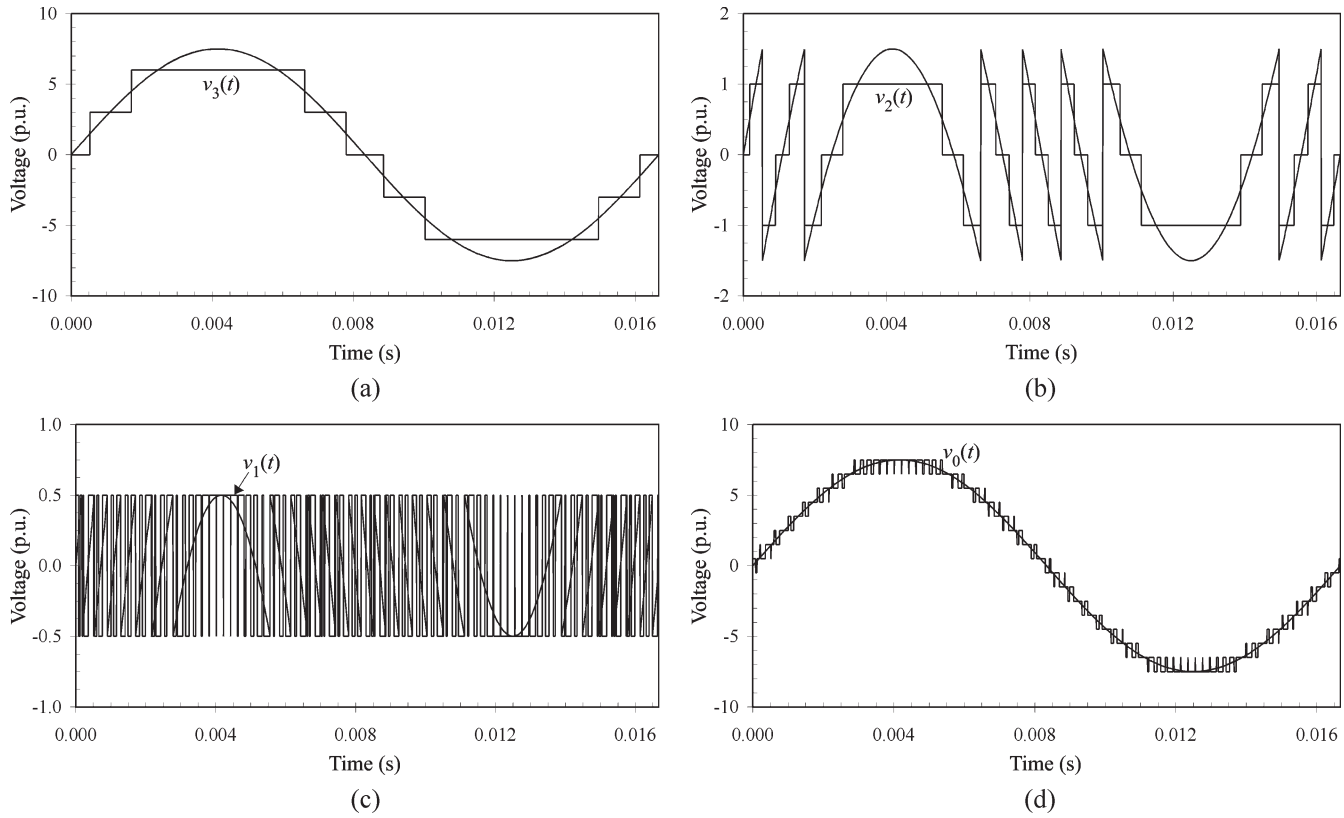


Fig. 5. Hybrid multilevel inverter with three distinct series-connected cells ($V_1 = V_2 = 1$ p.u., $V_3 = 3$ p.u., $m_a = 1$, and $f_1 = 4860$ Hz). (a) Cell 3. (b) Cell 2. (c) Cell 1. (d) Phase voltage.

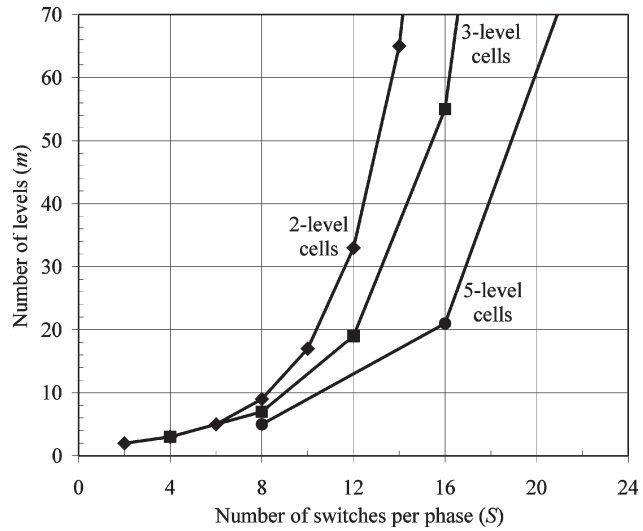


Fig. 6. Number of switching devices per phase versus maximum number of levels.

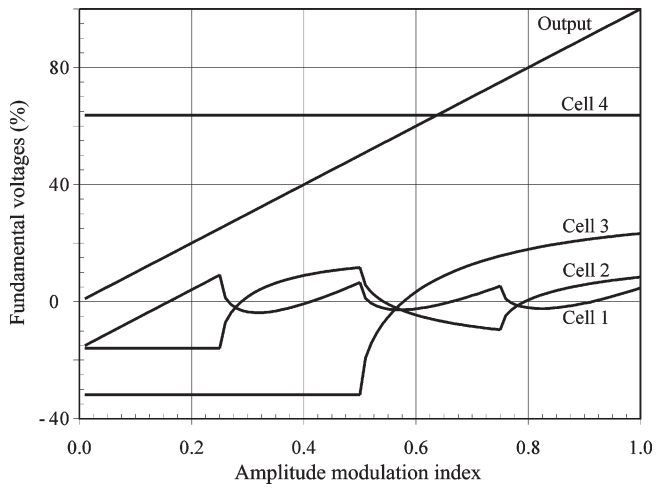


Fig. 7. Fundamental voltages synthesized by four two-level cells using the maximum voltage steps (Table I).

which is independent of the K_n value. This conclusion can be extended for any cell that synthesizes an even number of levels, as illustrated in Fig. 8(c) for a four-level cell. Consequently, although the excessive fundamental component is reduced with a larger number of levels, cells that generate an even number of levels should not be employed when it is desired to reduce the circulating energy at every operating point.

On the other hand, Fig. 8(b) and (d) demonstrates that three- and five-level highest power cells, respectively, synthesize the maximum fundamental voltage, without exceeding the fundamental output voltage for any m_a value, when $K_n = \pi/2$ [14]. Therefore, the highest power cell should be able to generate an odd number of levels, and its normalized voltage step should satisfy the following condition to reduce the circulating energy among the series-connected cells [15]:

$$V_n \leq \frac{\pi}{2}\sigma_{n-1}. \tag{18}$$

Lower power cells, which should synthesize an odd number of levels, can use the maximum normalized voltage steps (14)

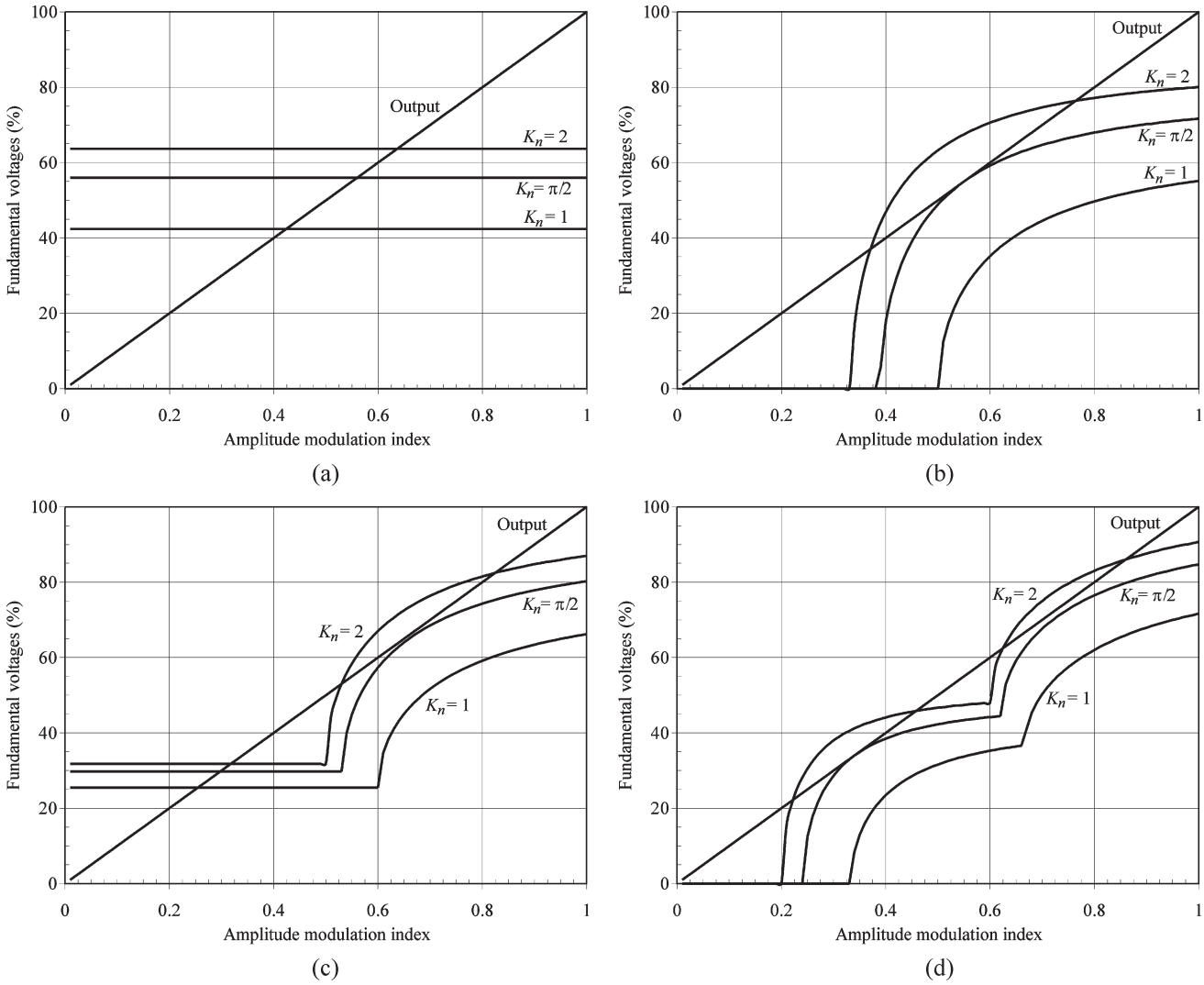


Fig. 8. Fundamental voltage synthesized by the highest power cell with different values of V_n. (a) Two-level cell. (b) Three-level cell. (c) Four-level cell. (d) Five-level cell.

because the excessive power levels processed by these cells are not significant when compared to the power amount processed by the nth cell.

Considering that all cells can generate an odd number of levels and the normalized voltage step of the highest power cell satisfy (18), Fig. 9 presents the number of levels synthesized by different hybrid multilevel inverters, using only three-, five-, or seven-level cells, by varying the number of switching devices per phase. This figure demonstrates that a larger number of levels can be obtained by using only three-level series-connected cells. Then, Fig. 10 shows the normalized voltage steps of the three-level cells, which are computed to satisfy the restrictions mentioned in this section to reduce the circulating energy among the cells [15].

C. Impact of the Topologies Used for Obtaining the DC Voltage Sources

Topologies adopted for implementing the isolated dc voltage sources in active power transfer applications affect the design methodology of a hybrid multilevel converter. For instance, when all dc sources are implemented with unidirectional rectifiers, it is not possible to regenerate energy from load to input source [17]. In this situation, series-connected cells cannot synthesize negative fundamental voltages for every operating point in motor mode (in the most critical case, for $0 \leq m_a \leq 1$), i.e., $V_{\text{fund},j} \geq 0$ for $j = 1, 2, \ldots, n$.

In order to satisfy this restriction, it is necessary that all cells synthesize voltage waveforms with fundamental components that are smaller than the output fundamental voltage. Consequently, all series-connected cells must be able to generate odd number of levels. Moreover, the voltage steps of all cells must be adequately determined as follows: As V_1 is equal to 1 p.u., it is necessary to find the maximum voltage step of the second cell that ensures that the lowest power cell does not synthesize a negative fundamental voltage when only these two cells are operating; next, the maximum value of V_3 should be computed to ensure that the two lower power cells do not synthesize a negative fundamental voltage when these three cells are operating. This principle can be extended to the nth

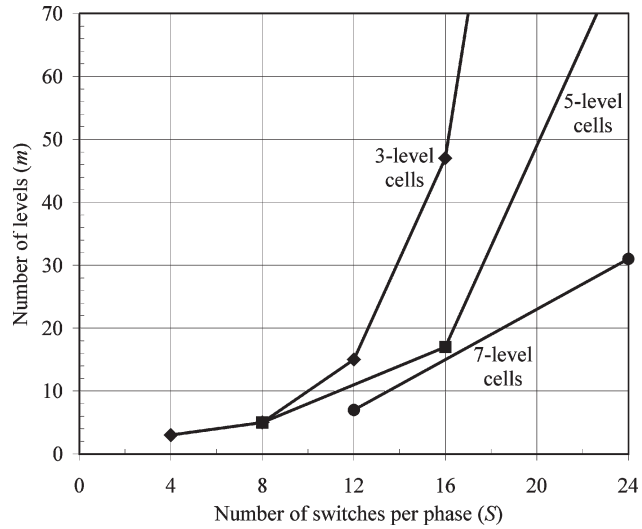


Fig. 9. Reduction of the circulating energy among the cells: number of switches per phase versus maximum number of levels.

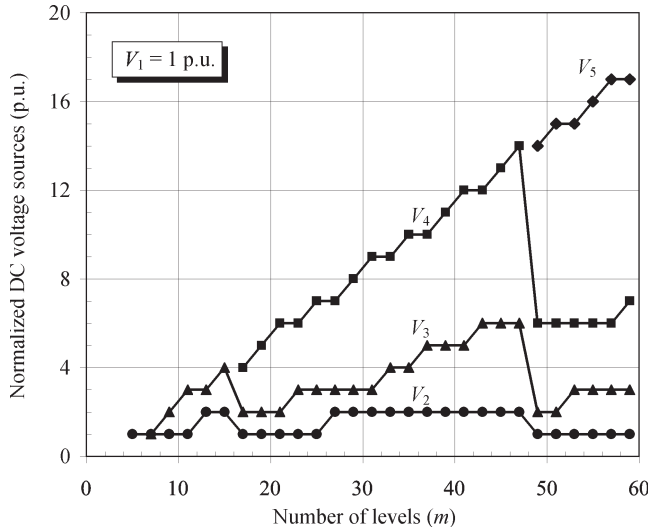


Fig. 10. Normalized voltage steps of series-connected three-level cells to reduce the circulating energy.

cell, obtaining the maximum number of levels that can be generated when unidirectional rectifiers are used in the input rectifier stage.

Table II shows the maximum number of levels that can be obtained in this case for distinct hybrid multilevel topologies, using only three-, five-, or seven-level cells connected in series. This table indicates that a larger number of levels can be generated by using only three-level cells. However, the same number of levels can be synthesized with five-level cells when 8 or 16 switches per phase are used. In addition, the two first cells of all arrangements with three-level cells operate with the same voltage steps. Thus, it is possible to replace them by a single five-level cell without decreasing the number of levels for a given number of switching devices.

As an example, Fig. 11 shows the simulation results of a hybrid multilevel inverter composed of a five-level lowest power cell in series with a three-level cell with 3-p.u. voltage steps.

With this topology, it is possible to obtain 11 voltage levels without regenerating energy for any m_a value, as shown in Fig. 12(a). On the other hand, using three-level cells with $V_1 = V_2 = 1$ p.u. and $V_3 = 3$ p.u. to generate the same 11 levels, Fig. 12(b) illustrates that the lowest power cell must handle with bidirectional power flow for some m_a range. Therefore, even presenting the same number of power devices and synthesizing the same number of levels, this configuration with three-level cells cannot be used when all input dc sources are implemented with diode rectifiers.

By increasing the number of switches per phase, those configurations using a five-level lowest power cell in series with three-level cells synthesize a larger number of levels than topologies employing only three-level cells. Table III presents the maximum number of levels obtained from these configurations, which can use unidirectional rectifiers at the input stage.

Therefore, from the desired number of levels and using Table III, it is possible to define the main parameters of a hybrid multilevel converter with uncontrolled rectifiers in the input stage.

D. Voltage Ratings of Semiconductor Devices

There can be applications in which the semiconductors used in one or more cells have already been defined by other factors, such as efficiency, cost, and availability off the shelf. Hence, there can be a limitation on the maximum voltage steps synthesized by some cells. Due to this fact, a generalized design methodology is proposed here, which also considers the voltage ratings of the semiconductor devices used in each cell. Such methodology is composed of eight basic points, as illustrated in the flowchart of Fig. 13.

I) Determine the minimum number of levels $m_{\min}$ of the hybrid multilevel inverter, using, for instance, the desired THD for the output voltages.

II) Compute the voltage base value $\Delta V_{\mathrm{dc},1}$, using the following equation:

$$\Delta V_{\mathrm{dc},1}(m) = \frac{2\sqrt{6}V_L}{3m_a(m-1)} \tag{19}$$

where V_L is the line rms output voltage, m_a is the nominal amplitude modulation index, and $m \geq m_{\min}$.

III) Determine the maximum normalized voltage steps of all cells $V_{\max,j}$ to ensure that voltage ratings of the switching devices will not be exceeded.

IV) According to the features of the application, find the configuration that synthesizes the desired number of levels with the smaller number of switches.

V) Determine the number of series-connected cells and voltage steps that synthesize the highest number of levels with this number of cells.

VI) Verify if the voltage steps obtained at Point V are smaller than or equal to the maximum normalized voltage steps computed at Point III. Two situations can occur.

a) The voltage steps obtained at Point V are smaller than or equal to the steps computed at Point III. Then, it is

TABLE II
COMPARISON AMONG HYBRID MULTILEVEL TOPOLOGIES THAT CAN USE UNIDIRECTIONAL RECTIFIERS IN ALL SERIES-CONNECTED CELLS

Switches per phase	Three-level cells		Five-level cells		Seven-level cells	
	m	*Topology*	*m*	*Topology*	*m*	*Topology*
8	5	2 cells ($V_1 = V_2 = 1$ pu)	5	1 cell ($V_1 = 1$ pu)	–	–
12	9	3 cells ($V_1 = V_2 = 1$ pu, $V_3 = 2$ pu)	–	–	7	1 cell ($V_1 = 1$ pu)
16	17	4 cells ($V_1 = V_2 = 1$ pu, $V_3 = 2$ pu, $V_4 = 4$ pu)	17	2 cells ($V_1 = 1$ pu, $V_2 = 3$ pu)	–	–
20	35	5 cells ($V_1 = V_2 = 1$ pu, $V_3 = 2$ pu, $V_4 = 4$ pu, $V_5 = 9$ pu)	–	–	–	–
24	73	6 cells ($V_1 = V_2 = 1$ pu, $V_3 = 2$ pu, $V_4 = 4$ pu, $V_5 = 9$ pu, $V_6 = 19$ pu)	53	3 cells ($V_1 = 1$ pu, $V_2 = 3$ pu, $V_3 = 9$ pu)	31	2 cells ($V_1 = 1$ pu, $V_2 = 4$ pu)

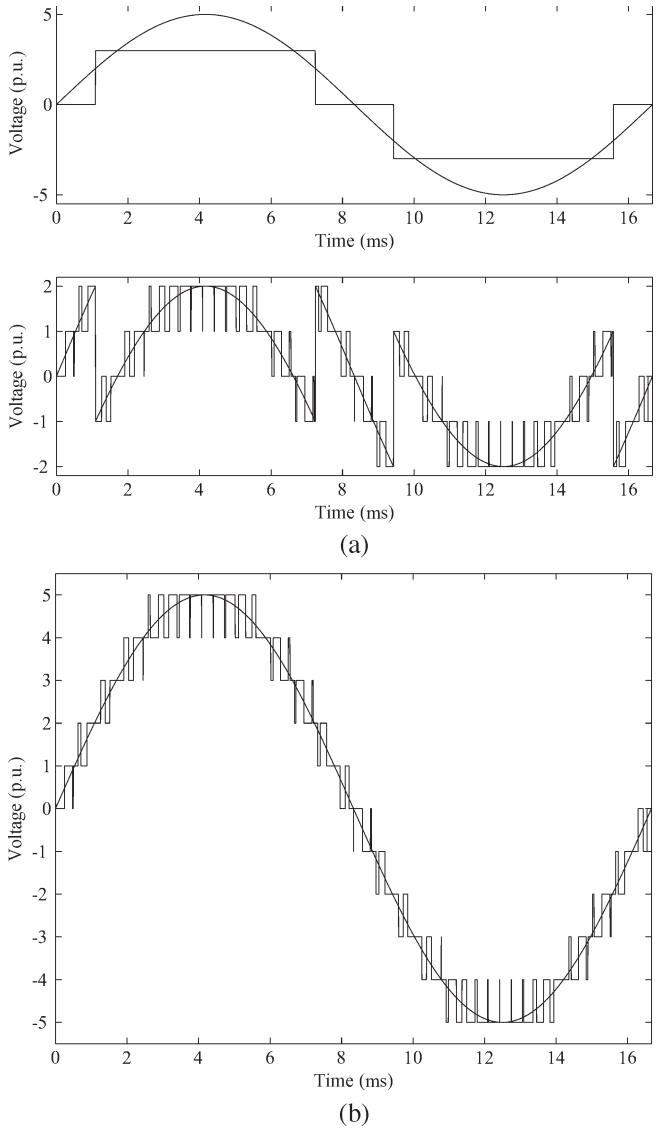


Fig. 11. Eleven-level hybrid inverter that is composed of a five-level cell ($V_1 = 1$ p.u.) in series with a three-level cell ($V_2 = 3$ p.u.). (a) Output voltages of series-connected cells. (b) Phase-voltage waveform.

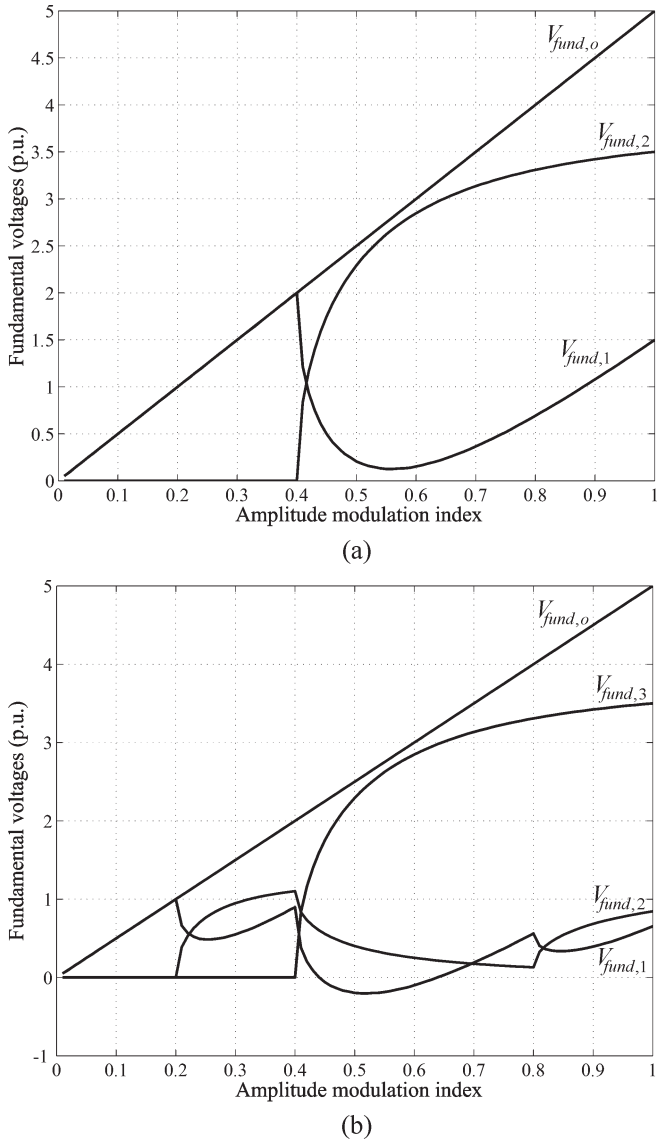


Fig. 12. Fundamental voltages. (a) Eleven-level hybrid inverter that is composed of a five-level cell ($V_1 = 1$ p.u.) in series with a three-level cell ($V_2 = 3$ p.u.). (b) Eleven-level hybrid inverter composed of three three-level cells connected in series ($V_1 = V_2 = 1$ p.u., $V_3 = 3$ p.u.).

possible to use the switches specified for each cell and to jump to Point VIII to finalize the design.

b) One or more voltage steps obtained at Point V are greater than the voltage steps computed at Point III. In this case, it is necessary to go to the next point since the configuration obtained from Points IV and V must be modified.

TABLE III
HYBRID MULTILEVEL INVERTERS THAT ALLOW TO USE UNIDIRECTIONAL RECTIFIERS IN ALL CELLS, USING A FIVE-LEVEL LOWEST POWER CELL IN SERIES WITH THREE-LEVEL CELLS

Switches per phase	Number of cells	Voltage steps	Number of levels
12	2	$V_1 = 1$ p.u., $V_2 = 3$ p.u.	11
16	3	$V_1 = 1$ p.u., $V_2 = 3$ p.u., $V_3 = 6$ p.u.	23
20	4	$V_1 = 1$ p.u., $V_2 = 3$ p.u., $V_3 = 6$ p.u., $V_4 = 12$ p.u.	47
24	5	$V_1 = 1$ p.u., $V_2 = 3$ p.u., $V_3 = 6$ p.u., $V_4 = 12$ p.u., $V_5 = 26$ p.u.	99

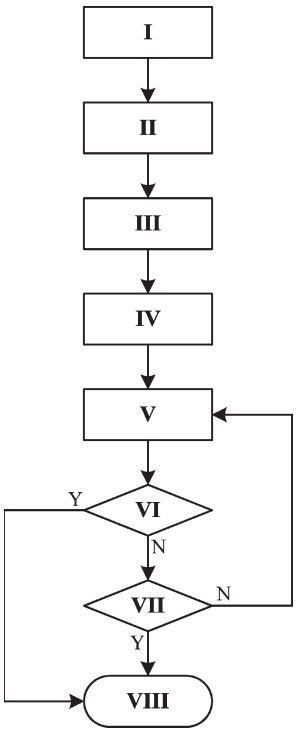


Fig. 13. Flowchart of the generalized design methodology.

VII) Decrease the voltage steps that are larger than the maximum normalized values, until they become equal, and verify if the resulting number of levels is larger than or equal to the minimum number of levels. Again, two situations can occur.
   a) The resulting number of levels is larger than or equal to the minimum number of levels. Therefore, it is possible to go to the next point.
   b) The resulting number of levels is smaller than the minimum number of levels. In this case, it is necessary to add another cell in series, using the same configuration of the highest power cell, and to return to Point V.

VIII) After defining the number of cells, the voltage steps that do not exceed the voltage ratings of semiconductor devices, and the resulting number of levels (larger than or equal to the minimum number of levels), adequate switching devices can be defined for each cell.

IV. DESIGN EXAMPLE

This section presents a practical design example of a hybrid multilevel inverter to be applied as a 4.16-kV adjustable-speed drive (at $m_a = 0.95$). All dc voltage sources must be implemented with unidirectional rectifiers, and the THD of the output line voltages, without any low-pass filter, should be smaller than 10% around the nominal operating point. In addition, it is specified that the voltage ratings of the switching devices should be smaller than 1700 V.

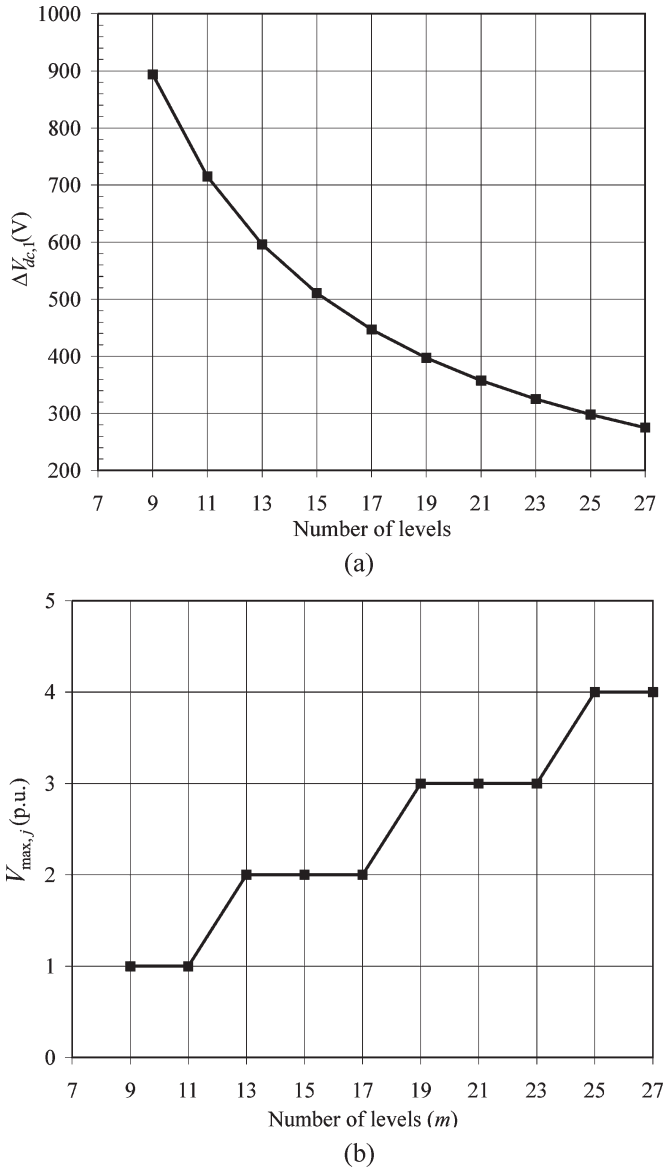
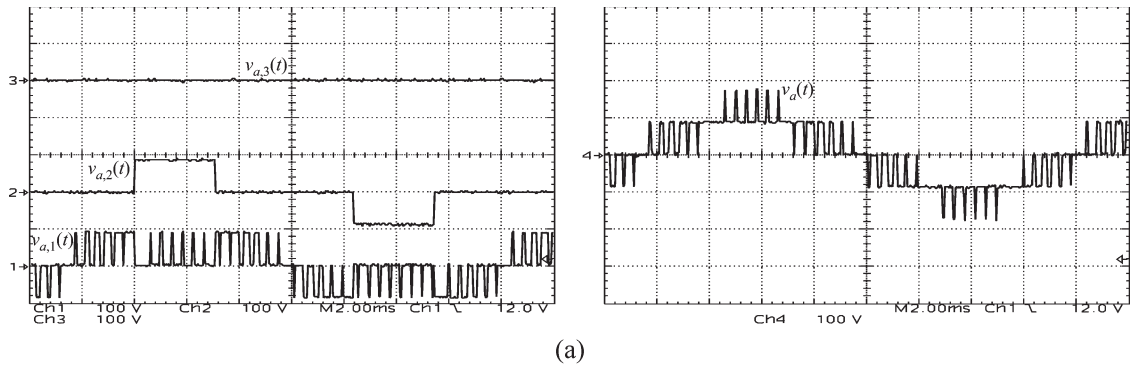
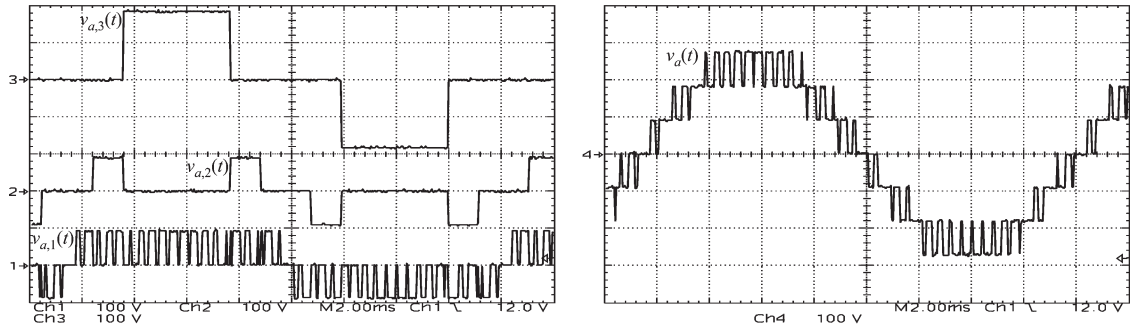


Fig. 14. Design example. (a) Voltage base value versus number of levels. (b) Maximum normalized voltage steps versus number of levels.

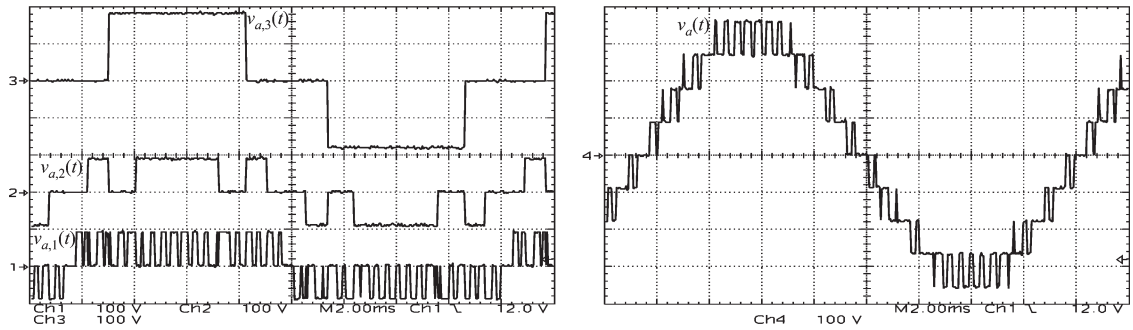
According to [15], the inverter should be able to synthesize phase voltages with nine distinct levels so that the THD of the



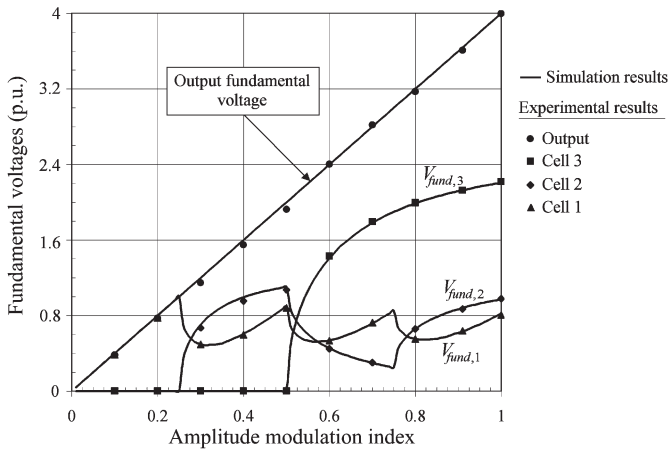
(a)



(b)



(c)



(d)

Fig. 15. Experimental results of a nine-level inverter that is composed of three three-level series-connected cells ($V_1 = V_2 = 1$ p.u. and $V_3 = 2$ p.u.): (left) output voltages of the series-connected cells and (right) output phase voltage. (a) $m_a = 0.3$. (b) $m_a = 0.7$. (c) $m_a = 0.91$ (nominal). (d) Fundamental voltages.

line voltages is smaller than 10% around the nominal point. In this example, $V_L = 4.16$ kV, and $m_a = 0.95$; then, it is possible to obtain the voltage base value, as shown in Fig. 14(a). The maximum normalized voltage steps of all cells $V_{\max,j}$ should be determined at Point III to ensure that the voltage ratings of the switching devices are not exceeded. Fig. 14(b)

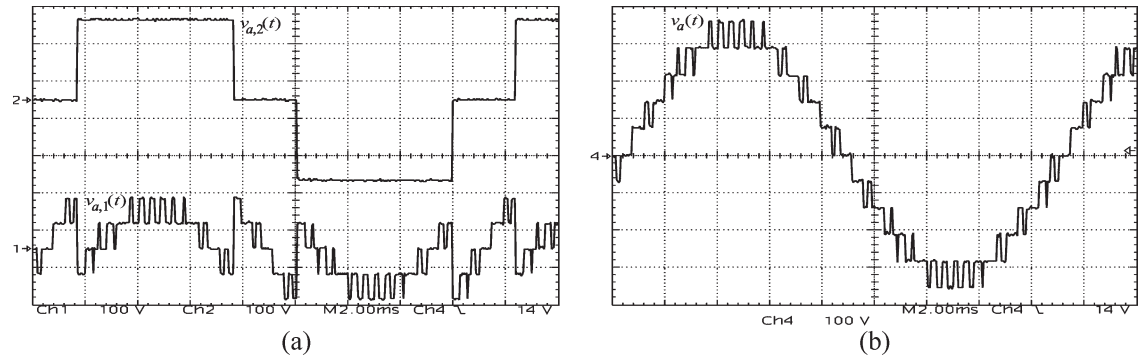


Fig. 16. Experimental results: eleven-level inverter that is composed of a five-level cell ($V_1 = 1$ p.u.) in series with a three-level cell ($V_2 = 3$ p.u.). (a) Output voltages of the series-connected cells. (b) Output phase voltage.

presents the maximum normalized voltage steps, considering in this example that the voltage ratings of the switches (1700 V) are, at least, 30% higher than the voltage steps synthesized by series-connected cells.

Points IV and V consist of determining an adequate configuration, which synthesizes the desired number of levels with the smallest number of switching devices. From Table II, it is possible to obtain nine phase-voltage levels by using three three-level cells with $V_1 = V_2 = 1$ p.u. and $V_3 = 2$ p.u. Nevertheless, 11 phase-voltage levels can be generated with 12 switches per phase, when the lowest power cell is able to synthesize five levels and the highest power cell synthesizes three levels with 3-p.u. voltage steps, as indicated in Table III.

However, with 11 voltage levels, it is necessary to decrease V_2 until 1 p.u., as represented in Fig. 14(b), so that it is possible to use 1700-V semiconductor devices. The resulting number of levels becomes smaller than the minimum number of levels, and it is necessary to add another three-level cell in series and to return to Point V of the design methodology. At this point, there are two three-level cells in series with a lowest power five-level cell. From Table III, the voltage steps that generate the maximum number of levels are $V_1 = 1$ p.u., $V_2 = 3$ p.u., and $V_3 = 6$ p.u., which result in 23 levels. Again, the voltage steps synthesized by some cells are larger than the maximum voltage step (3 p.u.). By decreasing V_3, the resulting number of levels also decreases, modifying $V_{\max,j}$ to 2 p.u. Then, the voltage ratings of switching devices are not exceeded when $V_2 = V_3 = 2$ p.u., resulting in 13 distinct voltage levels. Due to the fact that the three-level cells operate with the same voltage levels, it is possible to replace them by a single five-level cell, reducing the number of isolated dc voltage sources. Since $\Delta V_{\mathrm{dc},1} \approx 600$ V, the switching devices of the lowest power cell could be 1200-V insulated-gate bipolar transistors (IGBTs), such as BSM200GA120DLC from Eupec, while the switching devices of the highest power cell could be 1700-V IGBTs, such as BSM200GA170DLC from Eupec [19].

V. Experimental Results

Initially, a low-power prototype of a hybrid multilevel inverter with three series-connected H-bridge cells was built in our laboratory to demonstrate the operating principles of hybrid multilevel converters. Fig. 15 shows the output voltage waveforms of the three H-bridge cells, with voltage steps $V_1 = V_2 = 1$ p.u. and $V_3 = 2$ p.u., for distinct values of the amplitude modulation index. Fig. 15(c) presents the nine-level phase-voltage waveform ($\mathrm{THD} = 16.3\%$) synthesized by this multilevel converter at the nominal operating point. With these voltage steps and using the hybrid modulation strategy illustrated in Fig. 3(a), Fig. 15(d) demonstrates that the dc voltage sources can be implemented with unidirectional rectifiers.

On the other hand, it is possible to employ a five-level cell for the lowest power cell to synthesize a larger number of levels without increasing the number of switches, as shown in Table III. Fig. 16 presents the experimental results of a hybrid inverter that is able to generate 11 phase-voltage levels ($\mathrm{THD} = 12.8\%$), composed of a five-level high-frequency cell in series with a three-level cell synthesizing 3-p.u. voltage steps.

Both configurations use the same number of switching devices, and their dc voltage sources can be implemented with unidirectional rectifiers. However, the second arrangement can generate a larger number of levels by using a five-level topology for the lowest power cell.

VI. Conclusion

Asymmetrical multilevel converters are an alternative to minimizing the harmonic distortion of the output voltages without increasing the number of power devices. The use of different dc voltage values naturally leads to hybrid multilevel topologies, which employ distinct types of semiconductors and modulation strategies, in an effort to optimize the power processing of the overall system. On the other hand, these features increase significantly the flexibility and complexity of hybrid multilevel converter design.

To reduce this complexity, this paper included a comparative analysis among several hybrid topologies and proposed several design considerations for distinct applications to minimize the number of switching devices, to reduce the circulating energy among the series-connected cells, and to take into account the topology of the input rectifier stage and the voltage ratings of the switching devices. Consequently, by using the proposed design methodology, the number of series-connected cells, the dc voltage level and the number of levels of each cell can be defined to satisfy some design specifications.

Due to the enormous flexibility to design hybrid multilevel converters, this paper cannot cover all variables involved with them, but this paper provides an important basis to define an

adequate hybrid configuration for distinct systems. In the future, the results presented in this paper can also be extended to other hybrid multilevel modulation strategies, considering additional design specifications, such as weight/volume, efficiency, and other harmonic distortion factors.

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