Analog Integr Circ Sig Process (2011) 66:9–18
DOI 10.1007/s10470-010-9480-x

Very low input impedance low power current mirror

Hassan Faraji Baghtash · Seyed Javad Azhari

Received: 13 September 2009 / Revised: 14 April 2010 / Accepted: 5 May 2010 / Published online: 25 May 2010

Abstract In this paper a novel low input impedance current mirror/source is proposed. The principle of its operation compared to that of the simple current mirror is discussed. Also are given the comparative simulation results with HSPICE in TSMC 0.18 μm CMOS which verify the theoretical formulation and operation of the proposed structure. Simulation results show an input resistance for the proposed current mirror about 0.006 Ω. This is 4×10^5 times lower than that of the simple one while both working with 1.5 V supply and 50 μA bias current. It consumes only 161 μW and exhibits an excellent current error value of Zero at 55 μA which remains below 0.6% up to 100 μA. Favorably its minimum output voltage is reduced to 0.2 V.

Keywords Current mirror/source · Low input impedance · Low power · High accurate

1 Introduction

Current mirrors are one of the most important building blocks in electronic circuits and systems. They are used to perform current amplification, level shifting, biasing and loading. One of the major draw backs of conventional current mirrors is their rather high input impedance, while especially in current-mode signal processing the nodes impedances have to be very small. In fact this impedance has a substantial effect on overall dynamic range and frequency response of the circuit. There are many literatures dealing with the problems of input impedance [1–8]. In [1, 2] a voltage amplifier is inserted between the drain and gate of input transistor to decrease the input impedance. In [2] several possible implementations of the amplifier are studied. However these configurations suffer from poor stability problems. The better performance (35 Ω) is achieved in case of using a differential amplifier. The drawback of differential amplifier is that it needs high supply voltage and high power consumption [2]. The active input regulated cascode (AIRC) scheme reported in [3] uses differential amplifier in both input and output sides of current mirror. The used scheme is claimed to have very low input and high output resistance which is rejected in [4]. Moreover its input side loop contains two high impedance nodes which always require careful compensation to prevent both oscillations and transient response with long settling times. In [4] a current mirror is presented which achieves low input impedance (100 Ω) using flipped voltage follower (FVF) scheme. This scheme has some disadvantages as: transient and bandwidth performance degradation, circuit complexity, and higher power consumption. Moreover it requires carful design of biasing network. To improve the performance of this scheme some circuits are introduced in [5–7] which use two nested shunt feedback loops at the input side. One of them is implemented with a FVF and the other consists of an amplifier ($A1$) and a transistor (M1C). Both loops act simultaneously to reduce the input impedance. However these circuits can achieve too extremely low input impedances (0.75, 0.012 and 0.01 Ω respectively). But they all suffer from circuit complexity, higher power consumption, and offset current.

H. F. Baghtash · S. J. Azhari (✉)
Electronics Research Center, Electrical and Electronic Engineering Faculty, Iran University of Science and Technology (IUST), Tehran, Iran
e-mail: azhari@iust.ac.ir; sj_azhari@yahoo.com

H. F. Baghtash
e-mail: hfaraji@ee.iust.ac.ir

Furthermore in these circuits the feedback loop contains a very high impedance node which degrades input impedance frequency response. In other words their −3 dB cutoff frequency occurs in very low frequencies. The limitation of [5] is that in order to transistors MA1 and MA2 operate in saturation mode, V_{GS} of transistors M1C and M2C must be less than the threshold voltage of MA1 and MA2. This might not be possible in some CMOS technologies. Carful design of biasing network is required in [6] and circuit proposed in [7] uses floating gate transistors in its feedback loop which has its limitations and needs a more expensive technology to be implemented. In [8] the comparative study of various structures for amplifier placed in feedback loop are performed. In all these schemes the used amplifiers substantially add the complexity of the circuit and result in degradation in both band width and power consumption.

In recent decades current mode circuits have considerably attracted the attentions due to their highly demanded advantages [3, 9, 10]. Current mirrors are amongst the most used blocks of current mode circuits. They, hence, like current buffers and current operational amplifiers have to contain an input impedance as low as possible. As a current signal path, the lower is the input impedance of a current mirror the larger will be its efficiency in current transference to next stage. A Novel building block is therefore proposed here which significantly lowers the input impedance of current mirror while eliminating the offset biasing current, consumes low power and preserves other specifications. To get maximum efficiency out of this ultra low input impedance, the sheet resistance of related inter connections should also be reduced accordingly. Favorably the technology trend is encouragingly. In recent years the sheet resistance has decreased from 20 to 80 mΩ [11] to 5 mΩ [12] while elements density has passed 1 Billion per chip and is predicted to become more than 1000 Billions per chip in 2016 [13]. This trend however forces the layout engineers to devise even much lower sheet resistances. In fact, here is presented a current mirror to be able to face the challenges already imposed by technology and demands offered by consumers. In particular, it tends to be unique in this sense that can be connected to its previous block without interconnections!! This possibility arises from the point that most processors (especially current mode ones) contain a complementary output which includes PMOS transistor whose drain can be produced in common with the P type source terminal of M3 transistor (Figs. 1 and 2). This task which can be done by layout specialist eliminates the need for inter connections. Although here the principle of impedance reduction is shown on a simple current mirror, but other current mirrors also give the same result.

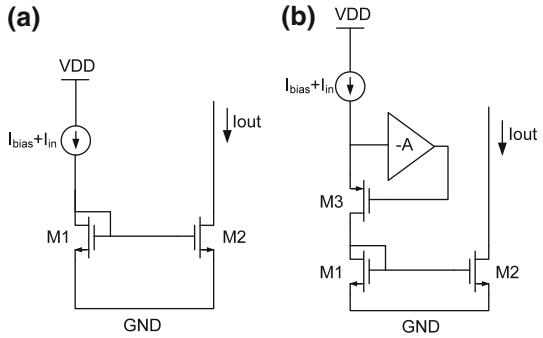

Fig. 1 **a** A simple current mirror; **b** a conceptual schematic of the proposed current mirror

2 The proposed low input impedance current mirror

The main idea is to incorporate transistor M3 in series with the input terminal of the basic circuit of the current mirror and use a gain amplifier of '$-A$' gain to control the gate voltage of M3. In Fig. 1 is shown a simple current mirror (a) and the conceptual schematic of the proposed current mirror (b). Any increment in source voltage of M3 (as the result of injected input current) causes its gate voltage to decrease '$-A$' times, hence causing stronger sink of input current which results in input impedance decrement by 'A'. Figure 2 shows transistor level implementations of this idea. As shown in Fig. 2(a) the amplifier can be implemented by only two transistors which act as a simple inverter for which input voltage is obtained as:

$$v_{in} = v_{sg3} + v_{ds4} \tag{1}$$

For the amplifier to have the significant gain required for perfect operation of the circuit, transistors M4 and M5 should operate in saturation region. If either of M4 or M5 leaves saturation condition, amplifier's gain reduces leading to increase of input impedance. The detailed analysis and formulation of the subject is given in Sect. 3.

Figure 2(b) shows another implementation of the added amplifier using self cascode scheme. By using self cascode schematic, effective length of transistors can be increased causing two advantages: (1) the gain of the amplifier increases due to increase of its output resistance hence leads to lower input resistance; (2) amplifiers' current is decreased which saves power consumption. The gain of amplifier can be increased by adding two extra cascode transistors. But this method has two limits; (1) supply voltage limits due to increasing of cascode transistors; (2) input impedance bandwidth degradation due to existing of a very high impedance node in feedback loop. Another scheme to achieve a higher gain is cascading of gain stages. Figure 2(c) shows a current mirror in which amplifier of "A" is implemented by cascading of a self cascode inverter of "$-A1$" gain and a positive gain stage of "$+A2$" building

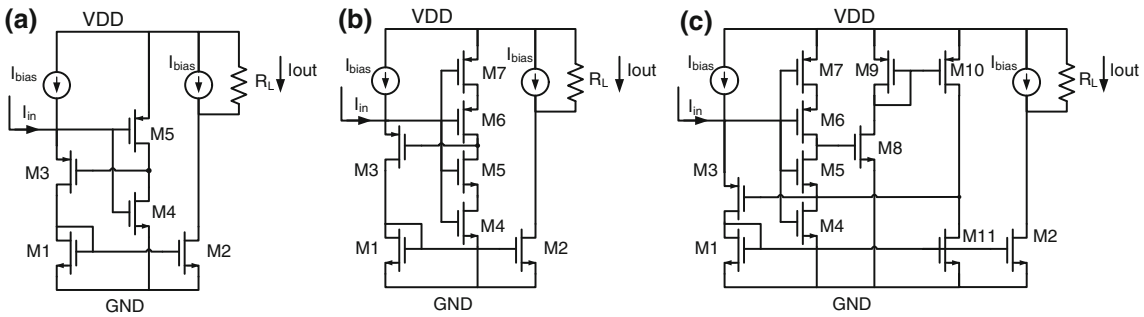

Fig. 2 Transistor implementation of the proposed current mirror

by transistors M8-M11. So the amplifiers gain of "*A*" obtains from (2) as:

$$A = A1 \times A2 \tag{2}$$

The advantage is that A can be increased without increase of power supply voltage.

3 Theoretical analysis of the proposed circuit

3.1 low frequency input resistance analysis

Figure 3 shows the small signal equivalent circuit for the proposed circuit (Fig. 2a) in which the direction of p-type current mirrors are drawn opposite to the direction of n-type ones to follow the behavior of the types of the transistors for the same V_{in}. By using Fig. 3 we get:

$$\left.\begin{aligned} v_{s3} = v_{g4} = v_{g5} = v_{in} \\ v_{s4} = v_{s5} = 0 \end{aligned}\right\} \xrightarrow{yields} v_{gs4} = v_{gs5} = v_{in} \tag{3}$$

$$\begin{aligned} v_{g3} &= -\left(g_{m4}v_{gs4} + g_{m5}v_{gs5}\right)\left(r_{ds4} \| r_{ds5}\right) \\ &= \left(g_{m4} + g_{m5}\right)\left(r_{ds4} \| r_{ds5}\right)v_{in} \end{aligned} \tag{4}$$

With reference to Fig. 2(a) we have:

$$A1 = -\frac{v_{g3}}{v_{in}} \tag{5}$$

which gives:

$$A1 = \left(g_{m4} + g_{m5}\right)\left(r_{ds4} \| r_{ds5}\right) = \frac{g_{m4} + g_{m5}}{g_{ds4} + g_{ds5}} \tag{6}$$

$$\begin{aligned} v_{in} &= I_{in}\left[\frac{1}{g_{m1}} \middle\| r_{ds1}\right] + \left(g_{m3}v_{gs3} + I_{in}\right)r_{ds3} \\ &\simeq I_{in}\frac{1}{g_{m1}} + \left(g_{m3}v_{gs3} + I_{in}\right)r_{ds3} \end{aligned} \tag{7}$$

$$v_{gs3} = \left(v_{g3} - v_{s3}\right) = -(A1 + 1)v_{in} \tag{8}$$

$$v_{in} = I_{in}\frac{1}{g_{m1}} - g_{m3}r_{ds3}(A1 + 1)v_{in} + I_{in}r_{ds3} \tag{9}$$

$$v_{in}(1 + g_{m3}r_{ds3}(A1 + 1)) = I_{in}\left[\frac{1}{g_{m1}} + r_{ds3}\right] \tag{10}$$

$$\begin{aligned} R_{in} = \frac{v_{in}}{I_{in}} &= \frac{\left[\frac{1}{g_{m1}} + r_{ds3}\right]}{1 + g_{m3}r_{ds3}(A1 + 1)} \simeq \frac{r_{ds3}}{1 + g_{m3}r_{ds3}(A1 + 1)} \\ &\simeq \frac{1}{g_{m3(A1+1)}} \end{aligned} \tag{11}$$

Performing same formulations for Fig. 2(b) and (c) to get R_{in} gives respectively:

$$R_{in} = \frac{1}{g_{m3}\left(\frac{g_{m4}+g_{m7}}{g_o} + 1\right)} \tag{12}$$

$$R_{in} = \frac{1}{g_{m3}\left(\frac{g_{m4}+g_{m7}}{g_o} \times \frac{g_{m8}g_{m10}}{g_{m9}\left(g_{ds10}+g_{ds11}\right)} + 1\right)} \tag{13}$$

where

$$g_o = \frac{g_{ds4}g_{ds5}}{g_{m5}} + \frac{g_{ds6}g_{ds7}}{g_{m6}} \tag{14}$$

3.2 Input impedance frequency response analysis

The frequency equivalent circuit for the proposed structure of Fig. 2(a) is shown in Fig. 4 in which we have:

$$\begin{aligned} c_{in} &= c_{gs4} + c_{gs5} + \left(c_{sd3} \| c_g\right) \\ c_{gdn} &= c_{gs3} + c_{gd4} + c_{gd5} \\ c_g &= c_{ds1} + c_{gs1} + c_{gs2} \end{aligned} \tag{15}$$

$$v_{gs4} = v_{gs5} = v_{in} \tag{16}$$

$$v_{g1} = \frac{I_{in}}{g_{m1} + g_{ds1}} \simeq \frac{I_{in}}{g_{m1}} \tag{17}$$

Now substituting I_{in} from (11) into (17) gives:

$$v_{g1} = \frac{1 + \frac{g_{m3}(A1+1)}{g_{ds3}} \times \frac{v_{in}}{g_{m1}+g_{ds1}}}{\left(\frac{1}{g_{m1}} + \frac{1}{g_{ds1}}\right)} \simeq \frac{g_{m3}A1}{g_{m1}}v_{in} \tag{18}$$

In (18) substituting $A1 \cdot V_{in}$ with $-V_{g3}$ as is noticed by (5) gives:

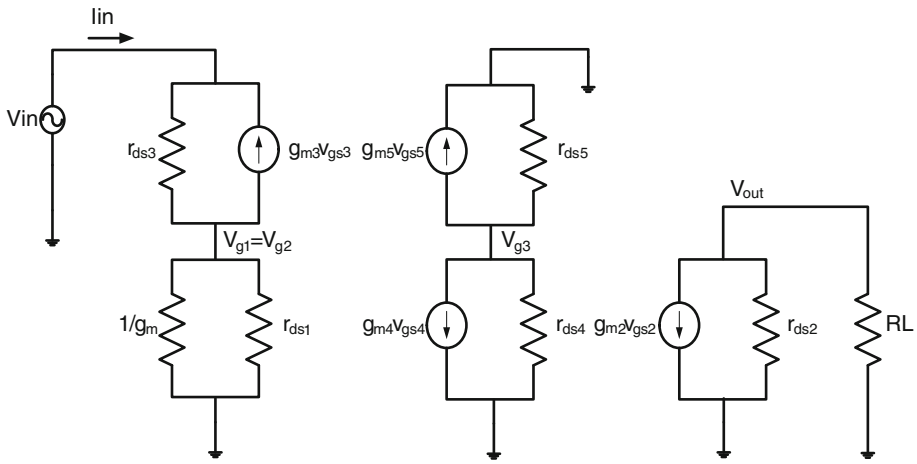

Fig. 3 Small signal equivalent circuit for proposed circuit (Fig. 2a)

$$v_{g3} = \frac{-g_{m1}}{g_{m3}} v_{g1} \tag{19}$$

By using Miller rules Fig. 4 can be simplified to Fig. 5 assisting to analyze input impedance as follows:

$$c'_{in} = c_{in} + (1 + A1)c_{gdn} \tag{20}$$

$$c'_g = c_g + \left(1 + \frac{g_{m2}}{g_l + g_{ds2}}\right)c_{gd2} + c_{gd3}\left(1 + \frac{g_{m1}}{g_{m3}}\right) \tag{21}$$

$$c_{dn} = \frac{c_{gd3}\left(1 + \frac{g_{m1}}{g_{m3}}\right)g_{m3}}{g_{m1}} + \frac{c_{gdn}(1 + A1)}{A1} \tag{22}$$

$$c_L = \frac{c_{gd2}\left(1 + \frac{g_{m2}}{g_L + g_{ds2}}\right)}{\frac{g_{m2}}{g_L + g_{ds2}}} + c_{ds2} \tag{23}$$

By defining y_n and y_1 as (24)

$$\begin{aligned} y_n &= g_{ds4} + g_{ds5} + sc_{dc} \\ y_1 &= g_{m1} + g_{ds1} + sc'_g \simeq g_{m1} + sc'_g \end{aligned} \tag{24}$$

We get:

$$I_{in} = \left(v_{in} - \frac{g_{m3}}{g_{ds3}} v_{gs3}\right)\left(\frac{g_{ds3} y_1}{g_{ds3} + y_1}\right) + sc'_{in} v_{in} \tag{25}$$

$$v_{gs3} = -\left(1 + \frac{g_{m4} + g_{m5}}{y_n}\right)v_{in} \tag{26}$$

Combining (25) and (26) gives:

$$v_{in}\left(1 + \frac{(g_{m4} + g_{m5} + y_n)g_{m3}}{y_n g_{ds3}}\right)\left(\frac{g_{ds3} y_1}{g_{ds3} + y_1}\right) + sc'_{in} v_{in} = I_{in} \tag{27}$$

By substituting y_1 and y_n from (24) in (27) we get for z_{in}:

$$\begin{aligned} z_{in} &\simeq \frac{\left(g_{m1} + sc'_g\right)(g_{ds4} + g_{ds5} + sc_{dn})}{B} \\ B &= \left(g_{m1} + sc'_g\right)[g_{m3} c_{dn} s + g_{m3}(g_{m4} + g_{m5})] \\ &\quad + sc'_{in}\left(g_{m1} + sc'_g\right)(g_{ds4} + g_{ds5} + sc_{dn}) \end{aligned} \tag{28}$$

which can also be arranged as:

$$\begin{aligned} z_{in} &\simeq \frac{a_0\left(1 + \frac{c'_g s}{g_{m1}}\right)\left(1 + \frac{c_{dn} s}{g_{ds4} + g_{ds5}}\right)}{b_0 + b_1 s + b_2 s^2 + b_3 s^3} \\ a_0 &= g_{m1}(g_{ds4} + g_{ds5}) \\ b_0 &= g_{m1} g_{m3}(g_{m4} + g_{m5}) \\ b_1 &= g_{m1}(g_{ds4} + g_{ds5})c'_{in} \\ &\quad + g_{m1} g_{m3} c_{dn} + g_{m3}(g_{m4} + g_{m5})c'_g \\ b_2 &= c'_{in} c'_g (g_{ds4} + g_{ds5}) \\ &\quad + g_{m3} c'_g c_{dn} + g_{m1} c_{dn} c'_{in} \\ b_3 &= c_{dn} c'_g c'_{in} \end{aligned} \tag{29}$$

Assume $c'_{in} > c_{dn}, c'_g$ and $g_{m1}, g_{m3} > g_{m4}, g_{m5}$ we get:

$$\begin{aligned} z_{in} &\simeq \frac{a'_0\left(1 + \frac{c'_g s}{g_{m1}}\right)\left(1 + \frac{c_{dn} s}{g_{ds4} + g_{ds5}}\right)}{b'_0\left(1 + b'_1 s + b'_2 s^2 + b'_3 s^3\right)} \\ a'_0 &= g_{ds4} + g_{ds5} \\ b'_0 &= g_{m3}(g_{m4} + g_{m5}) \\ b'_1 &= \frac{c_{dn}}{g_{m4} + g_{m5}} \\ b'_2 &= \frac{c_{dn} c'_{in}}{g_{m3}(g_{m4} + g_{m5})} \\ b'_3 &= \frac{c_{dn} c'_g c'_{in}}{g_{m1} g_{m3}(g_{m4} + g_{m5})} \end{aligned} \tag{30}$$

Or

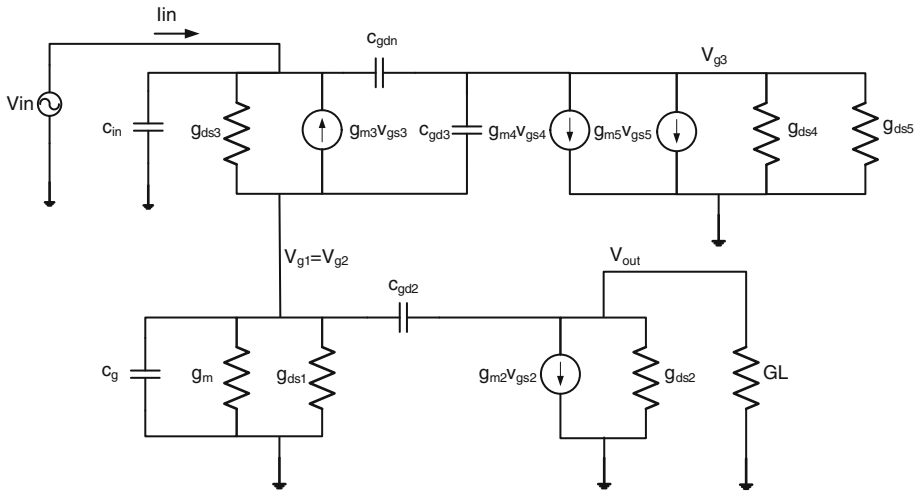

Fig. 4 High frequency equivalent circuit for proposed circuit (Fig. 2a)

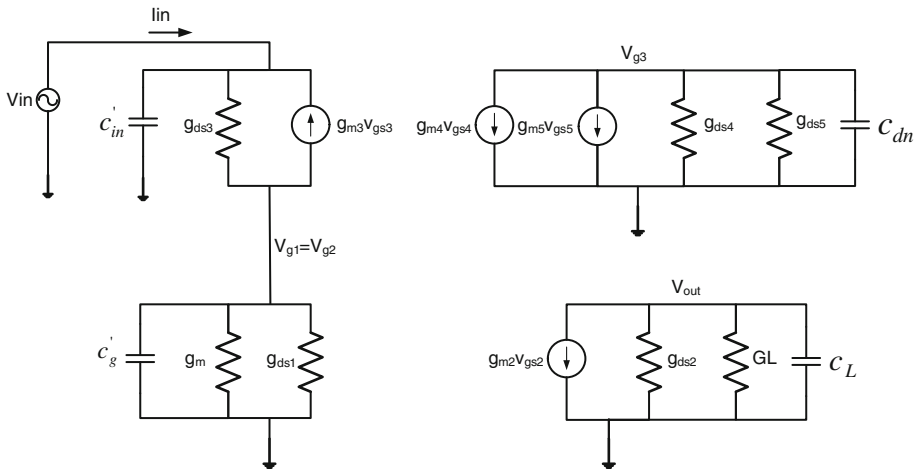

Fig. 5 Simplified high frequency equivalent circuit for proposed circuit (Fig. 2a)

$$z_{in} \simeq \frac{a'_0\left(1+\frac{c'_g s}{g_{m1}}\right)\left(1+\frac{c_{dn}s}{g_{ds4}+g_{ds5}}\right)}{b'_0\left(1+\frac{1}{p_1}s\right)\left(1+\frac{1}{p_2}s\right)\left(1+\frac{1}{p_3}s\right)} \tag{31}$$

Suppose $p_1, p_2 \ll p_3$ we get:

$$\frac{1}{p_1}\frac{1}{p_2}\frac{1}{p_3} = b'_3, \quad \frac{1}{p_1}\frac{1}{p_2} = b'_2 \overset{yields}{\longrightarrow} \frac{1}{p_3} = \frac{b'_3}{b'_2} = \frac{c'_g}{g_{m1}} \tag{32}$$

So (31) is simplified as:

$$z_{in} \simeq \frac{a'_0\left(1+\frac{c_{dn}s}{g_{ds4}+g_{ds5}}\right)}{b'_0\left(1+\frac{1}{p_1}s\right)\left(1+\frac{1}{p_2}s\right)} \tag{33}$$

If we assume $p_1 \ll p_2$ then we obtain:

$$\frac{1}{p_1}+\frac{1}{p_2} \simeq \frac{1}{p_1} = b'_1, \quad \frac{1}{p_1}\frac{1}{p_2} = b'_2 \overset{yields}{\longrightarrow} \frac{1}{p_2} = \frac{b'_2}{b'_1} = \frac{c'_{in}}{g_{m3}} \tag{34}$$

Comparing b'_1 (from (30)) to $\frac{b'_2}{b'_1} = \frac{c'_{in}}{g_{m3}}$ shows the rather equality of both values so that we can write:

$$\frac{c'_{in}}{g_{m3}} \simeq \frac{c_{dn}}{g_{m4}+g_{m5}} \Rightarrow \frac{1}{p_2} \simeq \frac{1}{p_1} \tag{35}$$

Relation (35) is against assumption $p_2 \gg p_1$ which should be corrected as $p_1 \simeq p_2$ leading to (36)

$$\frac{1}{p_1} \simeq \frac{1}{p_2} = \frac{1}{p} = \frac{b'_1}{2}, \quad \frac{1}{p_1}\frac{1}{p_2} = b'_2 \tag{36}$$

Substituting (36) into (33) gives:

$$z_{in} \simeq \frac{a'_0\left(1+\frac{1}{z}s\right)}{b'_0\left(1+\frac{1}{p}s\right)^2} = \frac{a'_0\left(1+\frac{c_{dn}s}{g_{ds4}+g_{ds5}}\right)}{b'_0\left(1+\frac{c_{dn}s}{2(g_{m4}+g_{m5})}\right)^2} = \frac{\left(1+\frac{c_{dn}s}{g_{ds4}+g_{ds5}}\right)}{g_{m3}(A1+1)\left(1+\frac{c_{dn}s}{2(g_{m4}+g_{m5})}\right)^2} \tag{37}$$

Relation (37) implies that z_{in} has two equal poles and one zero which are interrelated by $A1$ (specified by relation (6)) as is shown in (38):

$$p = 2A1 \times z \tag{38}$$

Relation (38) demonstrates a trade-off between input impedance value and its frequency response. Any increment in 'A' causes splitting between pole and zero to increase further which degrades the frequency response of z_{in}.

Performing same formulations for Fig. 2(b) gives:

$$A1c = \frac{g_{m4} + g_{m7}}{g_o} \tag{39}$$

and

$$z_{in} \simeq \frac{g_o\left(1 + \frac{c_{dn}s}{g_o}\right)}{b_0'\left(1 + \frac{c_{dn}s}{2(g_{m4}+g_{m7})}\right)^2} \tag{40}$$

where g_o is defined in (14). Now substituting (39) into (40) gives:

$$z_{in} \simeq \frac{\left(1 + \frac{c_{dn}s}{g_o}\right)}{g_{m3}(A1c + 1)\left(1 + \frac{c_{dn}s}{2(g_{m4}+g_{m7})}\right)^2} \tag{41}$$

And for Fig. 2(c) it gives:

$$\begin{aligned} A2 &= \frac{g_{m8}g_{m10}}{g_{m9}(g_{ds10} + g_{ds11})} \\ A &= A1c \times A2 = \frac{g_{m4} + g_{m7}}{g_o} \times \frac{g_{m8}g_{m10}}{g_{m9}(g_{ds10} + g_{ds11})} \end{aligned} \tag{42}$$

and

$$\begin{aligned} z_{in} &\simeq \frac{g_o(g_{ds10} + g_{ds11})\left(1 + \frac{c_g'S}{g_{m1}}\right)\left(1 + \frac{c_{dn1}S}{g_o}\right)\left(1 + \frac{c_{dn2}S}{(g_{ds10}+g_{ds11})}\right)}{b_0''\left(1 + b_1''S + b_2''S^2 + b_3''S^3 + b_4''S^4\right)} \\ &\simeq \frac{g_o(g_{ds10} + g_{ds11})\left(1 + \frac{c_{dn1}S}{g_o}\right)}{b_0''\left(1 + \frac{c_g'}{2g_{m1}}S\right)^2} \end{aligned} \tag{43}$$

Substituting (42) into (43) gives:

$$z_{in} \simeq \frac{\left(1 + \frac{c_{dn1}S}{g_o}\right)}{g_{m3}(A1c \times A2)\left(1 + \frac{c_g'}{2g_{m1}}S\right)^2} \tag{44}$$

where g_o is defined in (14) and:

$$\begin{aligned} b_0'' &= g_{m3}(g_{m4} + g_{m5})\left(\frac{g_{m8}g_{m10}}{g_{m9}}\right) \\ b_1'' &= \frac{c_g'}{g_{m1}} \\ b_2'' &= \frac{c_{dn1}c_{in}''g_{m9}(g_{ds10} + g_{ds11})}{g_{m3}g_{m8}g_{m10}(g_{m4} + g_{m5})} \\ b_3'' &= \frac{c_{dn1}c_{dn2}c_{in}''g_{m9}}{g_{m3}g_{m8}g_{m10}(g_{m4} + g_{m5})} \\ b_4'' &= \frac{c_{dn1}c_{dn2}c_{in}''c_g'g_{m9}}{g_{m1}g_{m3}g_{m8}g_{m10}(g_{m4} + g_{m5})} \end{aligned} \tag{45}$$

$$\begin{aligned} c_{in}'' &= c_{in} + (1 + A1)\left(c_{gd4} + c_{gd5}\right) + (1 + A)c_{gs3} \\ c_{dn1} &\simeq c_{ds5} + c_{ds6} + c_{gd4} + c_{gd5} + c_{gs8} + c_{gd8}\left(1 + \frac{g_{m8}}{g_{m9}}\right) \\ c_{dn2} &= c_{ds10} + c_{ds11} + c_{gd10} + c_{gd11} + c_{gs3} \end{aligned} \tag{46}$$

Equations (41) and (44) present input impedance of Fig. 2(b) and (c) respectively. Note that in relations (37), (41), and (44) the second order poles are complex but due to the fact that their imaginary parts are small compared to real parts, we thus neglect their imaginary part to simplify the relations.

The relations (37) to (44) show that the z_{in} of proposed circuit has one zero and two dominant poles. For all schemes, Zero occurs in lower frequencies than poles. It is proved that any increment in amplifier's gain reduces the input impedance but meanwhile causes the zero to move towards lower frequencies, thus further degrades the band width of the input impedance. It can also be found from (44) and (42) that the DC value of z_{in} of the structure of Fig. 2(c) is proposition to $\frac{1}{\sqrt{k_{M3}\cdot k_{M8}}\cdot V_A^3\cdot k_{inverter}}$ which implies that the larger are the aspect ratios of M_3, M_8 and the inverters' transistors, the smaller would be z_{in} of this structure, the point that is followed in selection of related aspect ratios. Moreover, some other factors are also affecting the value of z_{in} which have been regarded in this design too.

4 Simulation results and discussion

HSPICE simulations are carried on using TSMC 0.18 μm CMOS technology utilizing single 1.5 V power supply. The MOSFETs aspect ratios are given in Table 1. I_{bias} is taken as 50 μA on which the ac input current is superimposed as required. Since we intended signal path (processing) applications of current mirrors rather than their biasing applications thus we examined the frequency response of the proposed structure of Fig. 2(c) which is shown in Fig. 6 and exhibits relatively high frequency bandwidth of 577 MHz. However, for higher frequency applications the structure of Fig. 2(a) can be used with a bandwidth of 1.21 GHz, of course, in expense of a larger z_{in} which can be compensated by proper setting the related transistors aspect ratios yet preserving the high frequency operation. For the same reason (AC applications) z_{in} (instead of R_{in}) is examined at $I_{bias} = 50$ μA applying an ac input current I_{in} (holding up class A operation), giving the comparative results shown in Fig. 7, proving very small value of 5.8 mΩ at low frequencies for the structure of Fig. 2(c). It is about 4×10^5 times smaller than input impedance of simple current mirror in the same conditions. Although it increases at higher frequencies

Table 1 Transistors aspect ratio

MOSFET name	Aspect ratio			
	Simple	Figure 2(a)	Figure 2(b)	Figure 2(c)
M1	3.6 μm/0.54 μm	3.6 μm/0.54 μm	3.6 μm/0.54 μm	3.6 μm/0.54 μm
M2	3.6 μm/0.54 μm	3.6 μm/0.54 μm	3.6 μm/0.54 μm	3.6 μm/0.54 μm
M3	NA	36 μm/0.18 μm	36 μm/0.18 μm	36 μm/0.18 μm
M4	NA	0.36 μm/0.18 μm	0.27 μm/0.18 μm	0.27 μm/0.18 μm
M5	NA	10.8 μm/0.18 μm	0.9 μm/0.54 μm	3.6 μm/0.54 μm
M6	NA	NA	45 μm/0.54 μm	23.13 μm/0.54 μm
M7	NA	NA	27 μm/0.18 μm	0.9 μm/0.18 μm
M8	NA	NA	NA	5.4 μm/0.54 μm
M9	NA	NA	NA	0.9 μm/0.54 μm
M10	NA	NA	NA	0.9 μm/0.54 μm
M11	NA	NA	NA	0.9 μm/0.54 μm

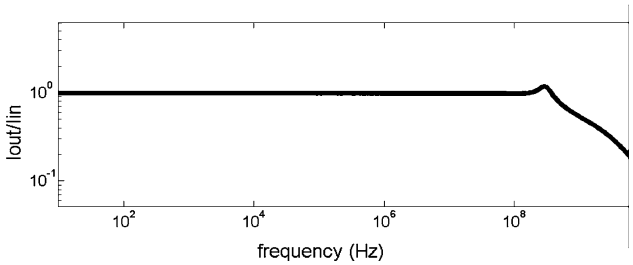

Fig. 6 Frequency response of proposed circuit shown in Fig. 2c

(with a Zero at ≈160 kHz) but still is smaller than that of simple current mirror inside the applicable unity gain bandwidth of both ones (cf. Figs. 6 and 7). However, the problem can be removed by either increasing zero frequency or/and decreasing poles frequencies (cf. Fig. 7 and relations (43) and (14)). This can be accomplished by a proper frequency compensation technique or suitable aspect ratios and capacitance values (especially C_{gs} ones) of related transistors. It should be noted that beyond f_T the performance of both the simple current mirror and the proposed ones degrades by fast reduction of λ ($\lambda = I_o/I_{in}$) makes of no importance the attempts may be expected for frequency improvement of z_{in} beyond f_T. The transient response of the proposed circuit (Fig. 2c) is checked by applying a current step by amplitude of 100 μA. The result is shown in Fig. 8. Figure 9 shows the output current when applying a sinusoidal current signal in the input node which also proves the stability of the proposed circuit. Favorably the minimum output voltage of the proposed current mirror is reduced to 0.2 V at class A operation (Fig. 10) which promises a high swing at output. By the same figure the average value of output impedance (z_o) of the proposed structures is measured as 407 kΩ at 50 μA (in the deep saturation region of Fig. 10). The current transfer error of the structure of Fig. 2(c) against bias current is shown in Fig. 11. It is measured about −0.07% at 50 μA, becomes about zero at 55 μA and keeps the same slope (of ≈0.14% per 10 μA) up to 250 μA at

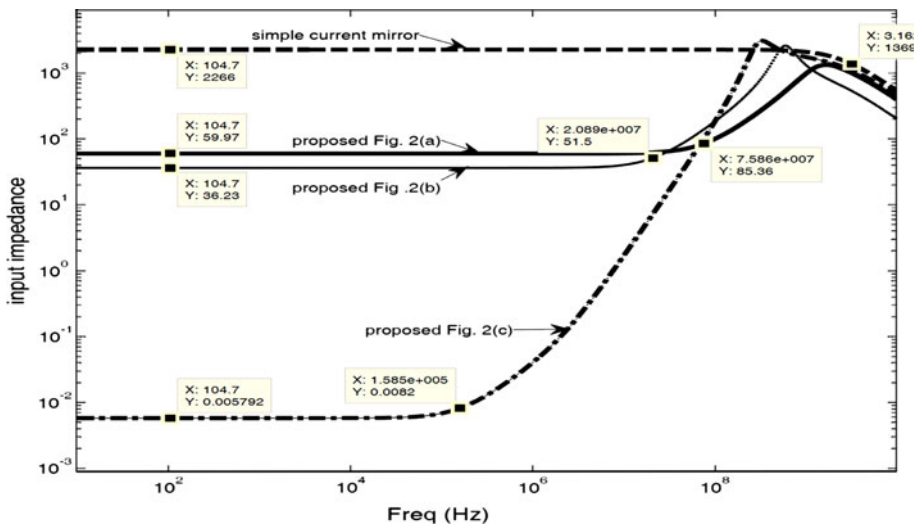

Fig. 7 High frequency input impedance of the proposed circuits compared to that of simple current mirror

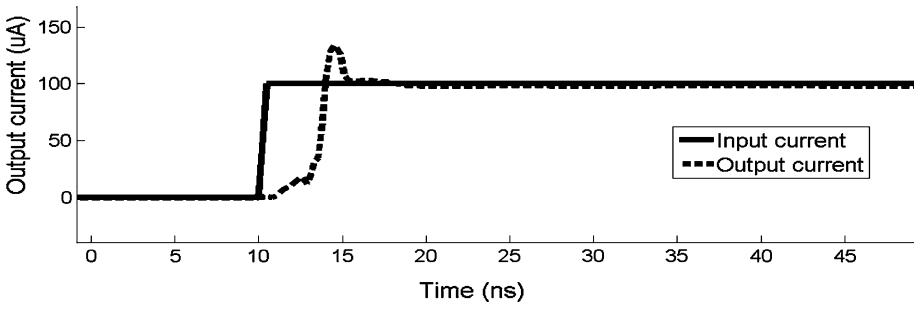

Fig. 8 Transient response of Fig. 2(c) (stability test)

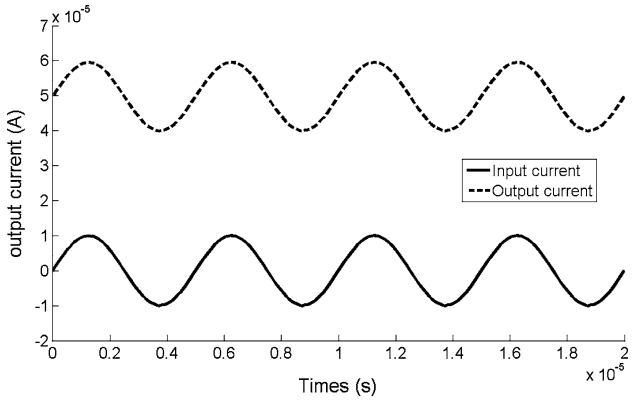

Fig. 9 The response of Fig. 2(c) to a sinusoidal input current (stability test)

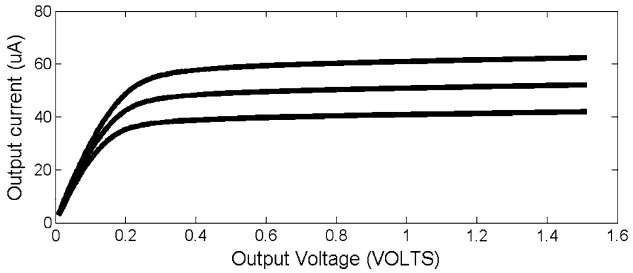

Fig. 10 Output current in terms of output voltage in class A operation

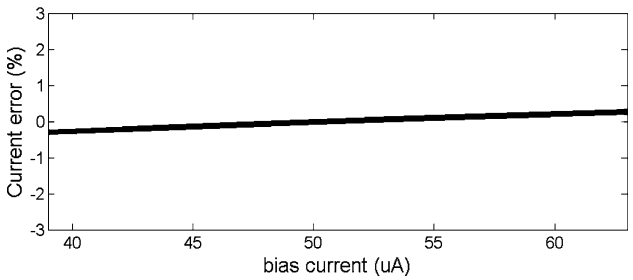

Fig. 11 Current transfer error

which reaches $\approx +10$ μA. for a more precise study of the overall behavior of the proposed current mirror its transfer function (I_{out} versus I_{in}) is plotted in Fig. 12 compared with that of the simple current mirror. The plot shows that both

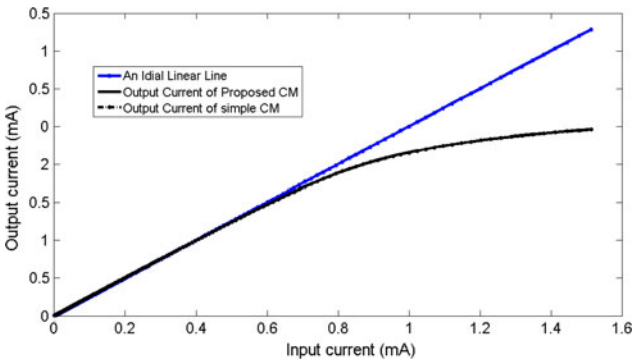

Fig. 12 Transfer function of the proposed current mirror (I_{out} vs. I_{in}) compared with that of simple current mirror

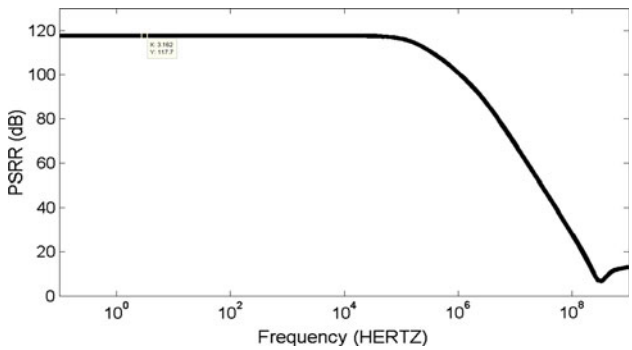

Fig. 13 PSRR of $A1cA2$; $A1cA2/(\Delta V_o/\Delta V_{DD})$

responses are exactly the same so that one cannot be distinguished from another. It also shows the high capability of the proposed current mirror in handling currents as large as 1.5 mA and more. The plot shows the same slope as of an ideal linear line (which is drawn for comparison) up to currents about 0.65 mA which can be taken as the minimum dynamic range of the proposed current mirror. This range can be extended to 0.93 mA for applications tolerating errors up to 10%.

To investigate the gain of the amplifiers ($A1cA2$) used in the structure of Fig. 2(c) versus "V_{DD}" variations the PSRR of $A1cA2$ as is defined in [8], i.e. ($A1cA2/(\Delta V_o/\Delta V_{DD})$), is evaluated and shown in Fig. 13. In this definition "V_o" is the output voltage of the second amplifier fed back to the gate of M3 for which we have: $V_o = V_{D11} = V_{G3} = A1cA2\ V_{in}$.

Table 2 Comparative results

Reference	Simple	[8]–Fig. 2(e)	This work		
			Figure 2(a)	Figure 2(b)	Figure 2(c)
DC power (μW)	113	198	187	154	161
DC offset (nA)	0.01	NA	0.01	0.01	0.01
Input Impedance	2.27 kΩ	27.7 Ω	60 Ω	36 Ω	~6 mΩ
	$1/g_m$	$2/(g_m^2 r_o^3)$	$1/(g_m A1)$	$1/(g_m A1c)$	$1/(g_m A2 A1c)$
Output impedance (kΩ)	407	2300	407	407	407
	r_o	$g_m^2 r_o^3$	r_o	r_o	r_o
BW (MHz)	2340	1280	1210	492	577
$V_{in,min}$	0.6	NA	0.9	0.9	0.7
	V_{GS}	V_{dsat}	$V_{GS} + V_{dsat}$	$V_{GS} + 2V_{dsat}$	$V_{GS} + V_{dsat}$
Current transfer error (%)	−0.07 at $I_{bias} = 50$ μA	0.3 at $I_{bias} = 50$ μA	−0.07 at $I_{bias} = 50$ μA	−0.07 at $I_{bias} = 50$ μA	−0.07 at $I_{bias} = 50$ Ma, min. Zero at 55 μA, max. 10 μA at 250 μA
I_{bias} (μA)	50	50	50	50	50
PSRR (dB)	–	49.48	–	–	118
Supply voltage (V)	1.5	1	1.5	1.5	1.5
	$V_{GS} + V_{ds}$	$V_{SG} + V_{ds} + V_{ov}^{max}$	$\max(2V_{GS}, V_{GS} + 2V_{ds})$	$\max(2V_{GS}, V_{GS} + 2V_{ds})$	$\max(2V_{GS}, V_{GS} + 2V_{ds})$
Minimum output voltage	0.2 V	0.4 V	0.2 V	0.2 V	0.2 V
	V_{dsat}	$2V_{dsat}$	V_{dsat}	V_{dsat}	V_{dsat}
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm

$A1$, $A2$, and $A1c$ are defined in relations (6), (42), and (39) of the current paper, respectively

It thus represents the effect of the feedback loop on the input signal of the proposed current mirror. The resulted PSRR is about 118 dB reflecting the extremely small effect of "V_{DD}" variations on "V_{G3}" proving the high insensitivity of feedback loop (as a whole) to "V_{DD}" variations. Compared results are summarized in Table 2. To have a fair comparison the results of the proposed structure are compared with the F.B. Pseudo-amplifier contained structure of Fig. 2(e) in [8] which is introduced as the best one by the authors of that paper [8].

5 Conclusion

A novel structure to improve conventional current mirror's input impedance is introduced. The principle of the input impedance reduction is discussed. A comparison between the features of the proposed current mirror and the simple current mirror is presented both in analytic and simulation format. It is shown that input impedance is reduced significantly compared to that of the simple current mirror (in the order of 4×10^5 times). Current transfer error as another most important parameter in current-mode processing (and signal path application) reaches Zero at 55 μA and remains below 0.6% up to 100 μA. Simulation results in TSMC 0.18 μm CMOS technology with HSPICE are presented to demonstrate the performance validation of the proposed current mirror. As is shown the proposed current mirror achieves ultra low input impedances without degrading other specifications.

References

1. Nairn, D. G., & Salama, C. A. T. (1990). Current mode algorithmic analog-to-digital converters. *IEEE Journal of Solid State Circuits, 25*, 997–1004.
2. Yuan, F., & Sun, B. (2002). A comparative study of low-voltage CMOS current-mode circuits for optical communications. In *Circuits and systems, 45th midwest symposium on IEEE* (Vol. 1, pp. I-315–I-319), August 2002.
3. Serrano, T., & Linares-Barranco, B. (1994). The active input regulated cascode current mirror. *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Application, 41*(6), 464–467.
4. Ramírez-Angulo, J., Carvajal, R. G., & Torralba, A. (2004). Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 51*(3), 124–129.
5. Ramirez-Angulo, J., Sawant, M. S., Lopez-Martin, A., & Carvajal, R. G. (2005). Compact implementation of high performance CMOS current mirror. *Electronics Letters, 41*(10), 3–4.
6. Sawant, M. S., Ramírez-Angulo, J., López-Martín, A. J., & Carvajal, R. G. (2005) New compact implementation of a very high performance CMOS current mirror. In *Circuits and systems, 48th midwest symposium on IEEE* (Vol. 1, pp. 840–842), 7–10 August 2005.

7. Garimella, A., Garimella, L., Ramirez-Angulo, J., López-Martín, A. J., & Carvajal, R. G. (2005). Low-voltage high performance compact all cascode CMOS current mirror. *Electronics Letters, 41*(25), 1359–1360.
8. Hassen, N., Gabbouj, H. B., & Bsebes, K. (2009). Low-voltage high-performance current mirrors: Application to linear voltage-to-current converter. *International Journal of Circuit Theory and Applications.* doi:10.1002/cta.618.
9. Toumazou, C., Lidgey F. I., & Haigh, D. (Eds.). (1993). Analog IC design: The current-mode approach. Peter Peregrinus Ltd. on behalf of IEE, UK. Reprinted 1993.
10. Vidal, E., Alarcon, E., & Gilbert, B. (2004). Up-to-date bibliography of current-mode design. *Analog Integrated Circuits and Signal Processing, 38*, 245–262.
11. Weste, N., & Harris, D. (2005) CMOS VLSI design, Chapter 4 (3rd ed.). Addison Wesley.
12. MEMS and Nanotechnology Exchange. http://www.mems-exchange.org/catalog/P2080/.
13. International Technology Roadmap for Semiconductors. http://www.itrs.net/Links/2008ITRS/Update/2008_Update.pdf.

Hassan Faraji Baghtash was born in Miyandoab, Iran, in 1985. He received the BSc degree from Urmia University in 2007. He is currently pursuing his MSc study in Iran University of Science and Technology, Electrical and Electronic Engineering. His current research interests include current mode integrated circuit design, low voltage, low power circuit and systems and analog microelectronics.

Seyed Javad Azhari received the BSc degree in electronic engineering from Iran University of Science and Technology (IUST), Narmak, Tehran, the MSc degree in electronic instrumentation and measurement from Victoria University of Manchester, UK, and the PhD degree in electronics from UMIST, UK, in 1975, 1986, and 1990, respectively. He joined IUST as a Teaching and Research Assistant in 1975. At the same time, he had many part-time jobs in industries and governmental organization. He is the founder of Electronic Research Center (ERC) of IUST. Currently, he is an Associate Professor in electronic engineering (since 2001) working in Electrical Engineering Faculty and Electronic Research Center of IUST. He is interested in circuit and system design especially in current-mode field, electronic instrumentation and measurement, semiconductor devices and sensor technology. He is author of more than ten textbooks in electronics, author or coauthor of about twenty papers, and designer or co designer of many electronic instruments. He is a Member of the Iran Electrical Engineering Society and was the recipient of the O.R.S Award (UK) during 1987–1990.