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A novel ultra-high compliance, high output impedance low power very accurate high performance current mirror

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ABSTRACT

In this paper a novel ultra-high compliance, low power, very accurate and high output impedance current mirror/source is proposed. Deliberately composed elements and a good combination (for a mutual auto control action) of negative and positive feedbacks in the proposed circuit made it unique in gathering ultra-high compliances, high output impedance and high accuracy ever demanded merits. The principle of operation of this unique structure is discussed, its most important formulas are derived and its outstanding performance is verified by HSPICE simulation in TSMC 0.18 μm CMOS, BSIM3 and Level49 technology. Simulation results with 1 V power supply and 8 μA input current show an input and output minimum voltages of 0.058 and 0.055 V, respectively, which interestingly provide the highest yet reported compliances for current mirrors implemented by regular CMOS technology. Besides an input resistance of 13.3 Ω, an extremely high output resistance of 34.3 GΩ and −3 dB cutoff frequency of 210 MHz are achieved for the proposed circuit while it consumes only 42.5 μW and its current transfer error (at bias point) is the excellent value of 0.02%.

1. Introduction

Current mirrors are one of the essential widely used building blocks in analog integrated circuits. They are used to perform current amplification, biasing, active loading and level shifting. Hence, their efficient design improves the overall performance of the system. The most important parameters of current mirrors are accuracy, input/output compliances, input/output impedances, frequency bandwidth, linearity, noise and sensitivity to changes in load impedance. In many high performance applications, the performance of the simple current mirror is inadequate, especially due to low output resistance and high current transfer error. The traditional method to increase the output impedance and improve the accuracy is using cascode transistors to (equalize drain–source voltages of mirror transistors and) reduce channel length modulation effect. However cascoding the transistors increases the required supply voltage and decreases input/output compliances, which is not compatible with today's technology trend. Due to technology down scaling and its intrinsic benefits, the trend in VLSI design is to reduce voltage supply. Hence, low voltage and low power circuit designs are in great demand. It can be found that there are many researches dealing with methods to improve the performance of low voltage current mirrors. Some of these methods are based on using level shifters [1,2], FGMOS transistors [3,4] and bulk driven schemes [5–7]. Although these methods operate with low power supplies and maintain high compliances, but unfortunately they suffer from some drawbacks. Two first solutions introduce extra offset to the output current. Offset can be canceled using adaptive biasing, but at the cost of increasing power consumption and extra circuit complexity. FGMOS transistors suffer from charge entrapment during fabrication process, large capacitance DC biasing and special technology that requires higher design cost comparing to traditional transistors [8–10]. Moreover, they are not suitable for DC processing. Bulk driven current mirrors also suffer from current offset problem, low bandwidth, high power consumption and limitations imposed by implementation process [6].

One of most widely used current mirrors is the low voltage cascode one. It has moderately low input and high output impedances, moderately low input and output voltages and high accuracy. To further decrease its input voltage and impedance, the input current can be applied to the drain of the transistor M_1 [11] (Fig. 1a). However this method introduces some offset to the output current. This offset current can be eliminated by subtracting it from the input or the output node. However it increases the circuit's complexity and requires much more attention in the design of biasing network. The better solution is obtained using an amplifier to equalize the drain–source voltages of mirror transistors. The other advantage of this solution is that it also improves other specifications of current mirror such as input and output impedances. This method is implemented in [12–14]. In [12] in order to

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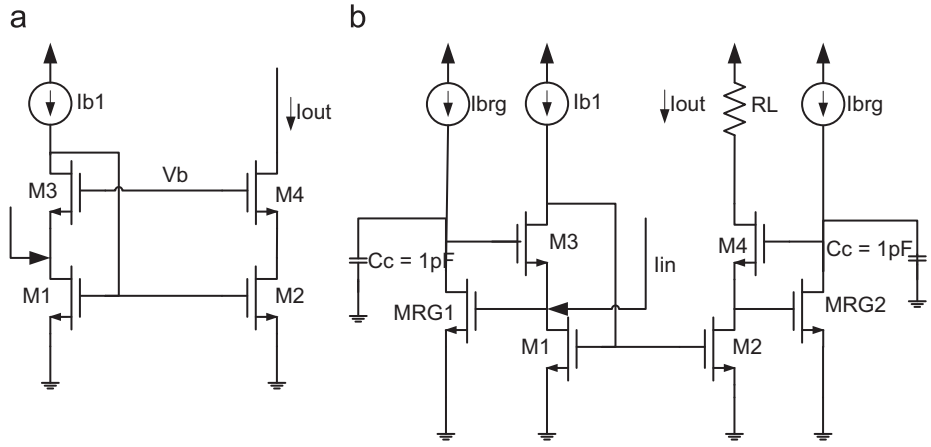

Fig. 1. (a) Low Voltage Cascode Current Mirror (LVCCM) and (b) regulated version of (a).

maintain M_{A1} and M_{A2} transistors in saturation mode of operation, V_{GS} of transistors M_{1C} and M_{2C} must be less than the threshold voltage of M_{A1} and M_{A2}. This may not be possible in some CMOS technologies. Careful designing of biasing network is required in [13] and circuit proposed in [14] uses floating gate transistors in its feedback loop, when its limitations were notified earlier. Moreover, all these circuits [12–14] suffer from complexity and their compliances are relatively low. Some recently reported simple and low voltage circuits are discussed in [15–17] in which their structures are as simple as low voltage cascode current mirror but their performance are inadequate in some applications where high output and low input impedances are needed [15].

In this work a novel high performance current mirror is presented that improves most of the aforementioned features acceptably. Simple structure of this current mirror gives a relatively high bandwidth and low power consumption. Its compliances are the highest yet reported for circuits implemented with regular CMOS technology, while exhibiting extremely low input and extremely high output impedance. Current dynamic range of the proposed current mirror is larger than that of low voltage cascode current mirror while maintaining a very high accuracy.

In Section 2 the proposed high performance current mirror is explained. Section 3 includes the HSPICE simulation results using TSMC 0.18 μm, BSIM3, Level49, CMOS technology and finally Section 4 concludes the paper.

2. Proposed high performance current mirror

2.1. Principle of operation

The proposed current mirror, conceptual schematic shown in Fig. 2, consists of a high swing cascode current mirror (M_1–M_4, with M_4 transistor connected as diode), M_5 as output transistor and an amplifier with gain amplitude of "$-A$". The high swing cascode is biased with $I_{b1}=I_{b2}=I_b$ currents and its input impedance is reduced using an FVF block [18] at input node and is driven by the input current signal I_{in}. Both cascode transistors M_3 and M_4 experience the same bias current; hence V_{ds1} is set equal to V_{ds2}, prohibiting the channel length modulation effect and thus a very high accurate result is attained. M_4, the diode connected cascode transistor, makes a separate biasing voltage source unnecessary. This transistor, on the other hand, provides the input and output nodes with an extra positive feedback loop, which increases the performance of the block without using extra circuitry. This structure includes two nested feedback loops in the input side. One of them is a negative shunt feedback implemented with an FVF

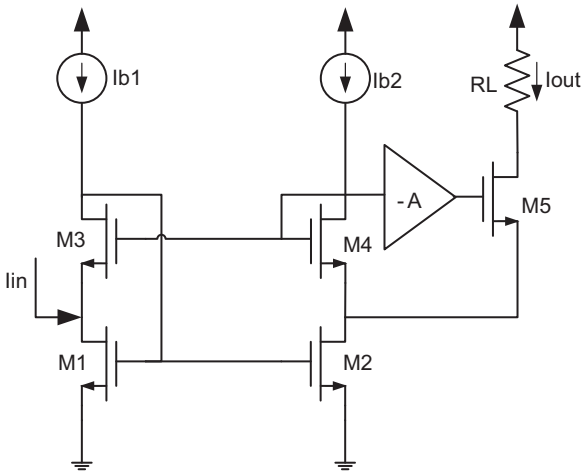

Fig. 2. Conceptual schematic of the proposed current mirror.

while the other one is a positive series type consisting of transistors M_1–M_4. Both loops act simultaneously and are specially devised to reduce the minimum input voltage, $v_{in,min}$, and the input impedance. Similarly, the output side includes two feedback loops, one of them is a negative series implemented by transistors M_4–M_5 and amplifier of "$-A$" and the next one is a positive shunt feedback consisting of transistors M_1–M_4. These two loops act simultaneously and are specially arranged to reduce the minimum output voltage, $v_{out,min}$, and increase the output impedance. In conventional method a negative series feedback is used to increase the output impedance. This reduces the output compliance by at least $1V_{dsat}$. In other word the feedback acts while the output voltage is greater than $2V_{dsat}$. By further decreasing the output voltage the feedback gain falls rapidly, causing the output impedance to be decreased rapidly due to the transistors entering the triode region.

Based on conventional definitions, MOS transistor linear region occurs when its output voltage becomes lower than $1V_{DS,sat}=V_{GS}-V_{GS,off}$ (i.e. $V_{DS}<V_{GS}-V_{GS,off}$), which leads to sharp reduction in output current versus voltage reduction. In other words for a transistor with constant V_{GS} voltage, the channel length modulation causes significant reduction in transistor output resistance. This means that I_{DS} becomes very sensitive to variation in V_{DS} in this region.

According to $I_{DS}=\beta(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$, the transistor current, I_{DS}, can be varied by both V_{GS} and V_{DS}. When transistor output voltage approaches to negative supply (here ground), then V_{DS} will

decrease causing reduction in transistor current (I_{DS}), of course if V_{GS} remains constant. Now consider the case that V_{GS} can be increased to a value, which despite of V_{DS} decrement, maintains the same I_{DS}. In such a case if it is arranged then makes the transistor current (I_{DS}) well robust against the output voltage variations. This is exactly what has arranged by the novel structure of the proposed current mirror (Fig. 2). Thanks to deliberately composed elements and well combined auto-controlled negative and positive feedback in the proposed circuit, which made it unique in the sense of gathering ultra-high compliances, high output impedance and high accuracy.

To explain the event in more detail, recalling the aforementioned descriptions about the nested feedbacks in the output node and supposing all transistors except M_1 and M_2 (which are always in triode region as will be discussed later) in saturation region, let us assume that due to some unwanted condition the output voltage is decreased from its initial value, then the principal of operation for the proposed circuit can be categorized in two parts: (1) M_5 is in saturation region and every variation in output voltage is extremely attenuated by negative feedback (related to M_5, M_4 and amplifier loop gain) that does not vary V_{d2}. In this condition the negative feedback is dominant and the output impedance will be maintained extremely high, which preserves the previous value of the output current (Fig. 3). (2) With further reduction in output voltage, M_5 will enter the triode region making the negative feedback much less effective; thus V_{d2} will trace the output voltage variation through M_5. In this condition the positive feedback dominates and will increase the $V_{GS1,2}$ voltage (due to the output voltage reduction) to compensate the I_{DS} deviation, thus keeping it constant (Fig. 3). In other words, since the constant current of I_{b2} flows through M_4, its gate voltage will follow V_{d2}, which then boosts the gate voltage of mirror transistors (M_1 and M_2) by means of M_3. The resulted increment in $V_{GS1,2}$, will compensate the reduction in I_{DS2}, which is caused by channel length modulation effect. In practice, although the transistor has been inevitably entered the linear region, but the aforementioned technique operates such that it keeps I_{DS} fixed by increasing $V_{GS1,2}$ so that we have $R_{out}=(\Delta V_{DS}/\Delta I_{DS})|_{\Delta I_{DS}=0}$, which makes the output impedance very large too. On the other side, in the proposed structure the embedded positive shunt feedback allows output voltage to approach to negative supply (here ground) meanwhile preserving its high output resistance and accurate current transfer features. It seems that the linear region boundary is shifted to lower output voltages, the greatly ever demanded event, now realized by this unique structure.

The conceptual description of the proposed method based on positive feedback is demonstrated in Fig. 3. Some recently proposed techniques used positive feedback schemes and gained high output impedance while achieving very low output voltages [19].

This is in fact a great achievement granted by special feedback arrangement and results a very wide dynamic range.

A very simple construction for gain amplifier suitable for the proposed current mirror of Fig. 2 is shown in Fig. 4. As shown it is implemented by only two transistors (configuring a self-cascode scheme) and a bias current of I_{bA}.

3. Circuit analysis

Analytical formulations to extract parameters of the proposed current mirror are performed in the following subsections, assuming that the source of each transistor is connected to its body. The simulations are also performed based on this assumption.

3.1. Output impedance analysis

In the following analysis, g_m, r_o and g_{ds} stand for the transconductance, the output resistance and the output conductance of the transistors. The transistors' numbers are indicated as subscripts of these parameters. Subscript "p" is also used to indicate "p" type transistors.

$$v_{out} = v_{d2} + v_{ds5} \tag{1}$$

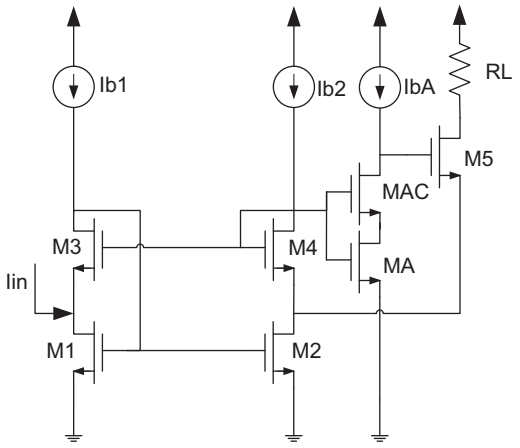

Fig. 4. Transistor implementation of the proposed current mirror.

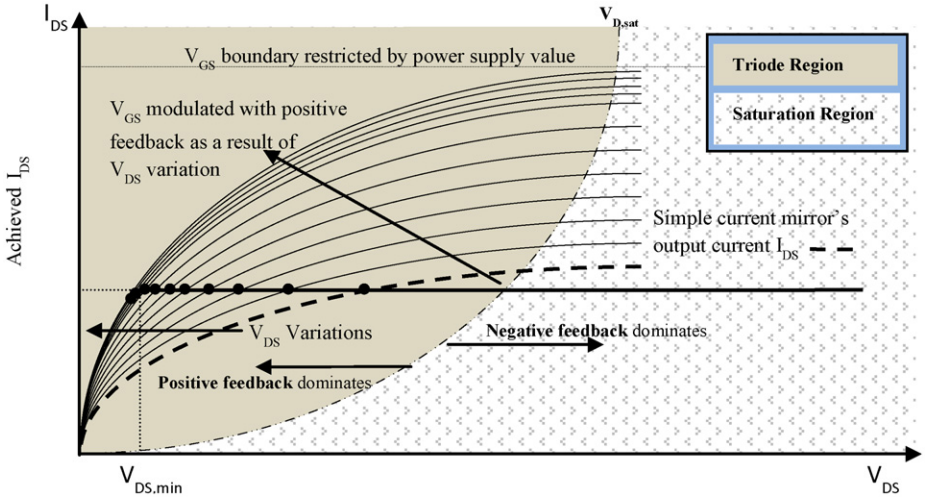

Fig. 3. Conceptual description of the proposed method based on positive feedback.

$$v_{ds5} = (I_{out} + g_{m5} v_{gs5}) r_{o5} \tag{2}$$

$$v_{gs5} = (A+1) v_{d2}$$
$$A \cong g_{mA} \left(\frac{g_{mAC}}{g_{dsA} g_{dsAC} + g_{dsbA} g_{mAC}} \| r_{obA} \right) \tag{3}$$

Substituting Eqs. (2) and (3) in Eq. (1) gives

$$v_{out} = v_{d2} + g_{m5} r_{o5} (A+1) v_{d2} + r_{o5} I_{out} \tag{4}$$

$$v_{d2} = (r_{ob2} \| r_{o2})(I_{out} - g_{m2} v_{d3}) \tag{5}$$

$$v_{d3} = -g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) (v_{g3} - v_{d1})$$
$$= -g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) (v_{d2} - v_{d1}) \tag{6}$$

$$v_{d1} = -\frac{g_{m1}}{g_{m3}} v_{d3} \tag{7}$$

Substituting Eq. (7) in Eq. (6) produces

$$v_{d3} = -g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) \left(v_{d2} + \frac{g_{m1}}{g_{m3}} v_{d1} \right) \tag{8}$$

This equation can be simplified as

$$v_{d3} = -\frac{g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1})}{1 + g_{m1} (r_{ob1} \| g_{m3} r_{o3} r_{o1})} v_{d2} \tag{9}$$

Substituting Eq. (9) in Eq. (5) gives

$$v_{d2} = -\frac{(r_{ob2} \| r_{o2})}{1 - \frac{g_{m2} g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) (r_{ob2} \| r_{o2})}{1 + g_{m1} (r_{ob1} \| g_{m3} r_{o3} r_{o1})}} I_{out} \tag{10}$$

Finally, substituting Eq. (10) in Eq. (4) gives

$$v_{out} = \left[r_{o5} + \frac{(1 + g_{m5} r_{o5} (A+1)) (r_{ob2} \| r_{o2})}{1 - \frac{g_{m2} g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) (r_{ob2} \| r_{o2})}{1 + g_{m1} (r_{ob1} \| g_{m3} r_{o3} r_{o1})}} \right] I_{out} \tag{11}$$

$$R_{out} = \left[r_{o5} + \frac{(1 + g_{m5} r_{o5} (A+1)) (r_{ob2} \| r_{o2})}{1 - \frac{g_{m2} g_{m3} (r_{ob1} \| g_{m3} r_{o3} r_{o1}) (r_{ob2} \| r_{o2})}{1 + g_{m1} (r_{ob1} \| g_{m3} r_{o3} r_{o1})}} \right] \tag{12}$$

Output impedance is then approximated as

$$R_{out} \cong \frac{g_{m5} r_{o5} (A+1) (r_{ob2} \| r_{o2})}{1 - \frac{g_{m2} g_{m3} (r_{ob2} \| r_{o2})}{g_{m1}}} \tag{13}$$

From Eq. (13) it is derived that the output resistance is capable to have negative or positive values. Also assuming ideal circumstances for the fabrication process an infinite resistance seems to be achievable by adjusting the transistors' aspect ratios. In most applications negative resistance is not required thus to avoid this condition, the following relation should be satisfied:

$$1 \geq g_{m3} (r_{ob2} \| r_{o2}) \tag{14}$$

In this work, Eq. (14) is satisfied by (1) making g_{m3} sufficiently small via choosing small $(W/L)_3$ and $(W/L)_4$ and (2) biasing M_1 and M_2 in their triode region, which cause r_{o1} and r_{o2} to be sufficiently small. These arrangements also help the current mirror to present high input and output compliances.

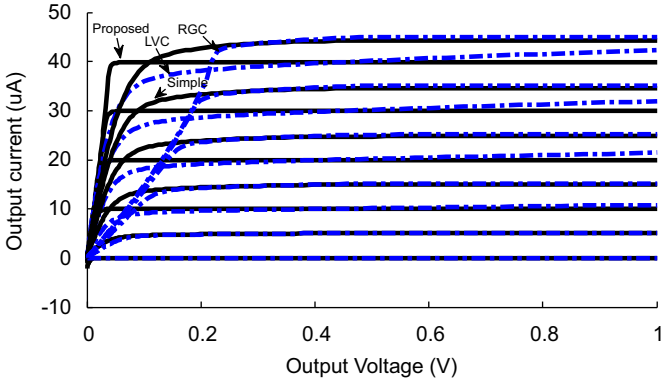

Fig. 6. I_{out} versus V_{out} (reflecting $g_{out} = R_{out}^{-1}$).

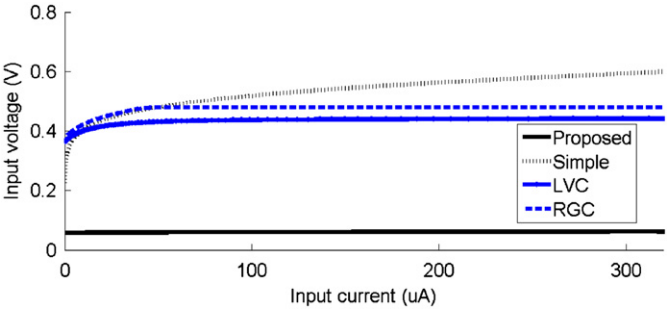

Fig. 7. V_{in} as a function of I_{in}.

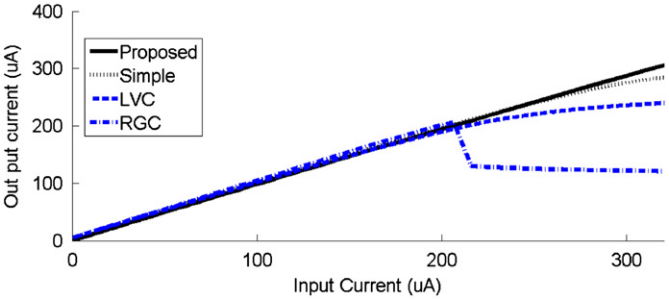

Fig. 8. Output current versus input current.

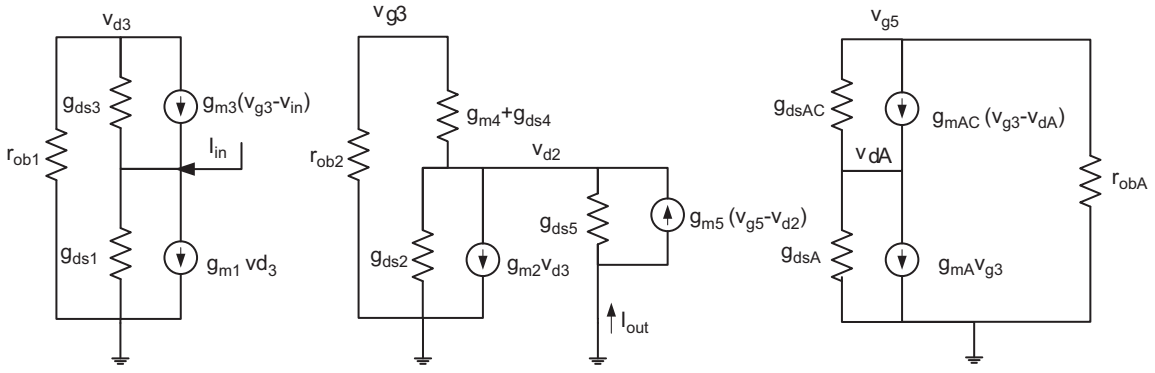

Fig. 5. Small signal equivalent circuit of the proposed current mirror ($v_{d3} = v_{gs1} = v_{gs2}$).

3.2. Input impedance analysis

$$I_{in} = g_{m1} v_{d3} + g_{ds1} v_{in} \tag{15}$$

$$v_{d3} = -g_{m3} (r_{ob1} \| \mu_3 r_{o1}) (v_{g3} - v_{in}) \tag{16}$$

$$v_{g3} = -\frac{g_{m1} v_{d3}}{g_{m5}(A+1)} \tag{17}$$

Substituting Eq. (17) in Eq. (16) gives

$$v_{d3} = \frac{g_{m3}^2 g_{m5}(A+1) v_{in}}{g_{m5}\, g_{ds3}\, g_{ds1}(A+1) - g_{m1} g_{m3}^2} \tag{18}$$

Substituting Eq. (18) in Eq. (15) gives

$$I_{in} = \left(\frac{g_{m1} g_{m3}^2 g_{m5}(A+1) v_{in}}{g_{m5} g_{ds3} g_{ds1}(A+1) - g_{m1} g_{m3}^2} + g_{ds1} \right) v_{in} \tag{19}$$

$$R_{in} = \frac{g_{m5} g_{ds3} g_{ds1}(A+1) - g_{m1} g_{m3}^2}{d1 + d2} \tag{20}$$

where

$$d1 = g_{m1} g_{m3}^2 g_{m5}(A+1)$$
$$d2 = g_{ds1} (g_{m5} g_{ds3} g_{ds1}(A+1) - g_{m1} g_{m3}^2) \tag{21}$$

The input impedance can be simplified as

$$R_{in} = \frac{g_{m5} g_{ds3} g_{ds1}(A+1) - g_{m1} g_{m3}^2}{g_{m1} g_{m3}^2 g_{m5}(A+1)} \tag{22}$$

The same as output resistance, it is proved in Eq. (22) that the input resistance can also get positive, zero and finally negative values just by adjusting transistors' aspect ratios. This ability makes the proposed circuit also well suited for some special applications where negative resistances are needed. On the other hand, to avoid negative input resistance wherever it is undesirable for the considered application, amplifiers' gain must be kept high enough, which also helps to decrease the input resistance (see Eq. (22)).

3.3. Current transfer analysis

Using KCL at input node (v_{in}) of proposed circuit (Fig. 5) and performing some approximations gives

$$I_{in} = v_{in}(g_{ds1} + g_{m3}) + v_{d3} g_{m1} - g_{m3} v_{g3} \tag{23}$$

Similarly using KCL at other nodes of proposed circuit results

$$I_{out} = v_{d2}(g_{ds2} + g_{m4}) + v_{d3} g_{m2} - g_{m4} v_{g3} \tag{24}$$

$$v_{d2} = \frac{r_{ob2} + (1/g_{m4})}{r_{ob2}}\, v_{g3} = v_{g3} \tag{25}$$

$$v_{in} = \frac{g_{ds3} + (1/r_{op1})}{g_{m1}} v_{d3} + v_{g3} \tag{26}$$

$$v_{g5} = \frac{I_{out}}{g_{m5}} + v_{d2} \tag{27}$$

$$v_{dA} = v_{g3} + \frac{(1/r_{obA}) + g_{dsAc}}{g_{mAc}} \tag{28}$$

$$v_{g5} = \frac{g_{mA} - g_{mAc}}{g_{dsAc}} v_{g3} + \frac{g_{mAc}}{g_{dsAc}} v_{dA} \tag{29}$$

Now substituting Eq. (28) in Eq. (29) and performing some simplifications, we obtain

$$v_{g5} = -g_{mA}\, r_{obA} v_{g3} \tag{30}$$

Substituting Eq. (29) in Eq. (27) gives

$$v_{d2} = \frac{I_{out}}{g_{m5}} - g_{mA} r_{obA} v_{g3} \tag{31}$$

Substituting Eq. (31) in Eq. (24) gives

$$v_{g3} = \frac{g_{ds2} + g_{m4} - g_{m5}}{g_{m5} g_{mA} r_{obA}\, (g_{ds2} + g_{m4})} I_{out} + \frac{g_{m2}\, v_{d3}}{g_{mA} r_{obA}\, (g_{ds2} + g_{m4})} \tag{32}$$

Substituting Eq. (25) in Eq. (31) gives

$$v_{g3} = \frac{I_{out}}{g_{m5}(1 + g_{mA} r_{obA})} \tag{33}$$

Substituting Eqs. (33) and (26) in Eq. (1) and performing some simplifications gives

$$I_{in} = g_{m1} v_{d3} + \frac{g_{ds1} I_{out}}{g_{m5}(1 + g_{mA} r_{obA})} \tag{34}$$

Substituting Eq. (33) in Eq. (32) and performing some simplifications give

$$v_{d3} = \frac{I_{out}}{g_{m2}} \tag{35}$$

Substituting Eq. (35) in Eq. (34) gives

$$\lambda = \frac{I_{out}}{I_{in}} = \frac{1}{1 + \frac{g_{ds1}}{g_{m5} g_{mA} r_{obA}}} \tag{36}$$

4. Simulation results

SPICE simulations are carried out using the TSMC 0.18 μm, BSIM3, Level49 and CMOS technologies with HSPICE utilizing single 1 V power supply. Load resistance, RL, of 3 kΩ is used. For all structures (simple, LV cascode, RGC and the proposed one) the aspect ratios of the transistors (if used) are M_1–M_2=45/0.54, M_3–M_4=4.5/0.27, M_5=36/0.18, M_A=0.9/0.18, M_{AC}=9/0.18, and M_{RG1}–M_{RG2}=0.9/0.54. Bias currents of I_b and I_{bA} are taken to have values of 5 and 2.5 μA, respectively. I_{in} is taken to have DC value of 15 μA. Fig. 6 shows the DC output characteristics with V_{out} swept from 0 to 1 V and I_{in} stepped from 0 to 40 μA in steps of 10 μA. As shown in this figure, the proposed circuit exhibits extremely

Table 1
Comparative results.

Reference	[16]	[17]	[12]	[13]	[14]	Simple	LVC (Fig. 1a)	RGC (Fig. 1b)	Proposed
I_{in} (μA)	50	50	NA	100	50	15	15	15	15
I_b (μA)	10	5	110	50	25	NA	5	5	5
$V_{in,min}$ (V)	0.14	0.23	NA	NA	NA	0.22	0.363	0.375	0.058
$V_{out,min}$ (V)	0.25	0.3	0.2 to 0.4	0.23 at I_{in}=10 μA	0.15	0.125	0.422	502	0.055
R_{in} (Ω)	1333	800	0.75	0.012	0.01	1266	266.6	333	13.3
R_{out} (Ω)	11 M	650 M	200 M	2.3 G	8 G	561 K	22.5 M	4.29 G	34.3 G
BW(MHz)	100	NA	620	220	200	270	340	270	210
Current transfer error (%)	NA	0.1	0.1	0.05	0.1	7	33	35	0.02
P (μW)	NA	NA	NA	NA	NA	30	40	50	42.5
V supply (V)	1.5	1.5	1.8	1.8	3	1	1	1	1
Technology	2 μm BSIM	0.35 μm HP	0.5 μm AMI	0.5 μm AMI	0.5 μm AMI	TSMC 0.18 μm	TSMC 0.18 μm	TSMC 0.18 μm	TSMC 0.18 μm

high output resistance of 34.3 GΩ along with much higher compliance voltage, which proves the good functionality of embedded positive feedback, making the structure suitable for ultra-low voltage applications. This figure also proves very high accuracy of output current together with negligible current offset, which makes the structure very preferable for modern ultra-high precision applications. Another more interested characteristic of current mirrors is dynamic range, which is depicted in Fig. 6 and validates the superior performance of proposed current mirror compared to other structures. Favorably the minimum input and output voltage of the proposed current mirror are reduced to 0.058 and 0.055 V, respectively, which promise ultra-high compliances at the input and the output nodes. Fig. 7 shows the input voltage as a function of input current. It is shown in Fig. 7 for a DC sweep of I_{in} from 1 to 300 μA, the maximum input voltage variation was found to be 4 mV. Following the same type of measurements performed in [12,13], the aforementioned values correspond to an approximate input resistance of 13.3 Ω, which is also another merit of the proposed current mirror. This figure also proves the capability of the proposed circuit to operate at extremely low input voltages. Fig. 8 shows the output current versus input current sweep. It is shown that the current dynamic range of the proposed current mirror is wider than that of all other current mirrors, i.e. simple, LVC and RGC current mirrors, which are included in the simulations. Favorably the current transfer error is achieved to be as low as 0.02%. The total power consumption of the proposed current mirror is about 42.5 μW. The compared results are summarized in Table 1. For simulating the practical fabrication condition, the Monte Carlo analysis is performed applying 5% mismatch in transistors' aspect ratios and threshold voltage with Gaussian distribution. The Monte Carlo simulation results are shown in Figs. 9–12. To further investigate the performance of the proposed circuit against PVT (process, VDD and temperature) variations, it is also simulated for various temperatures and supply voltages. The results are depicted in Figs. 13–18. These figures show that the fabrication process does not have significant effect on proposed circuit's performance, which is another excellent achievement.

The frequency response, the input voltage versus the input current and the output voltage versus the output current for various temperatures of −25, 0, 25, 50 and 75 °C are depicted in Figs. 13–15.

The output current transient response applying sinusoid input current of "$15u+1u\sin(2\pi\times 210\times 1E+6t)$" is shown in Fig. 16. The input voltage versus the input current and the output current versus the output voltage applying ±10% variations in power supply voltage are shown in Figs. 17 and 18, respectively.

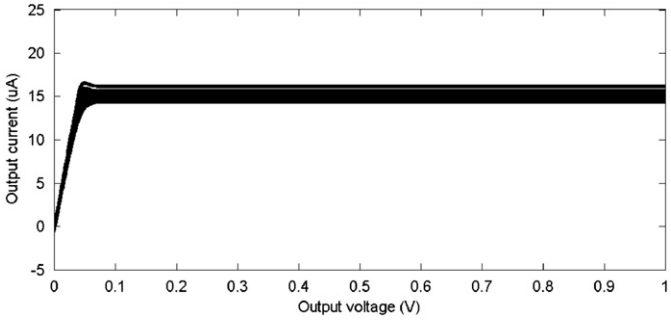

Fig. 11. Output current in terms of output voltage.

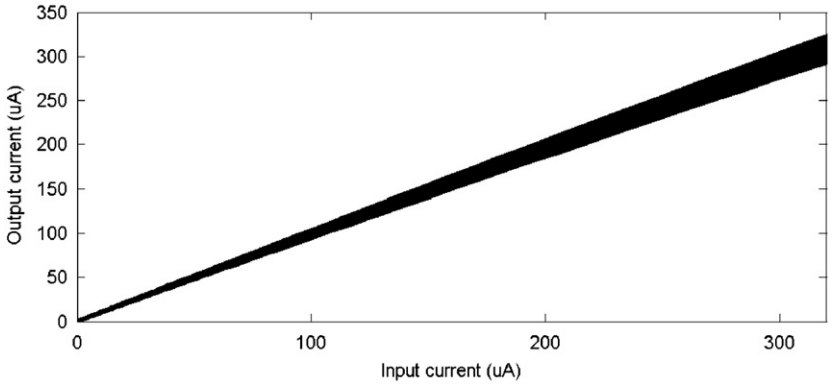

Fig. 9. Output current in terms of input one.

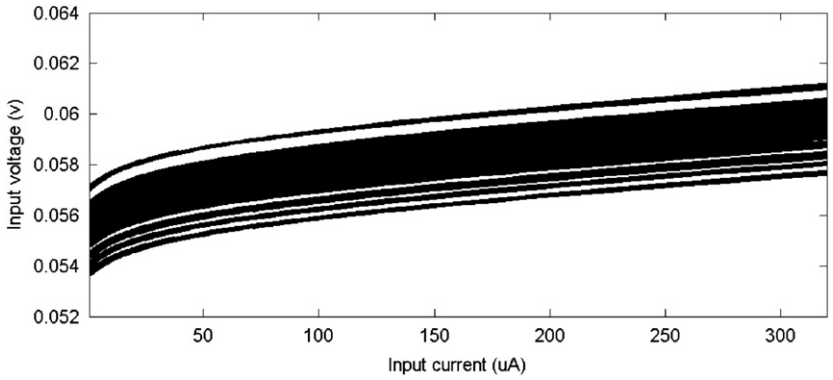

Fig. 10. Input voltage versus input current.

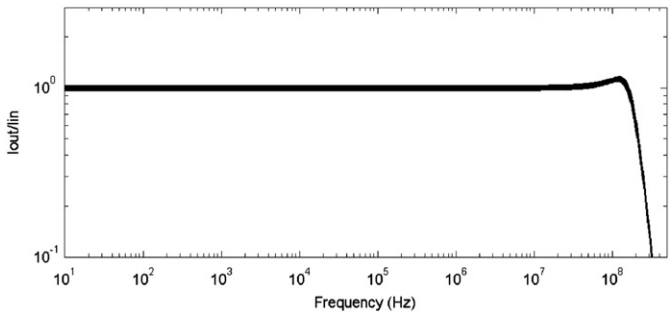

Fig. 12. Frequency response of the proposed CM.

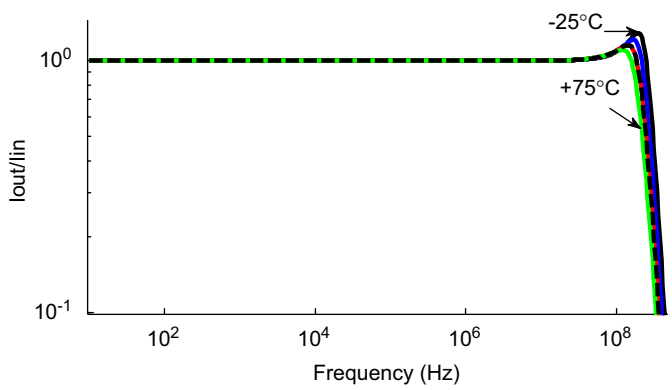

Fig. 13. Frequency response for various temperatures of −25, 0, 25, 50 and 75 °C.

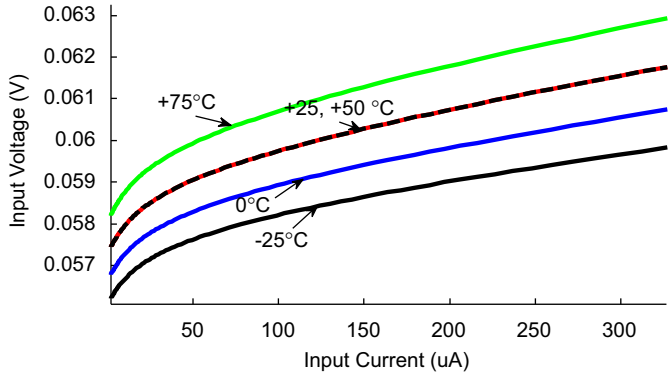

Fig. 14. Input voltage versus input current for various temperatures of −25, 0, 25, 50 and 75 °C.

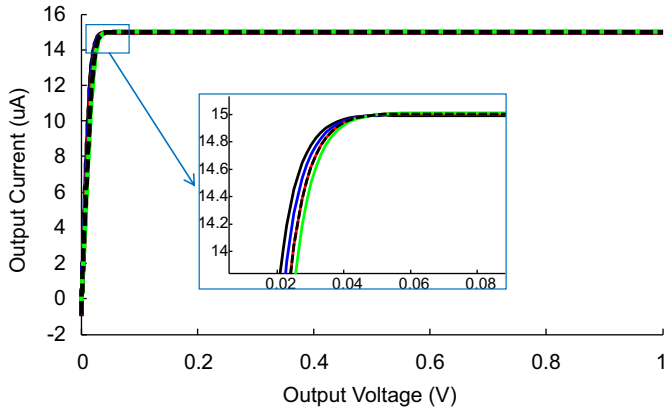

Fig. 15. Output voltage versus output current for various temperatures of −25, 0, 25, 50 and 75 °C.

5. Conclusion

A novel ultra-high compliance, very accurate and high output impedance current mirror is presented. As shown the proposed current mirror has a very low voltage and consumes very low power. Moreover it is very simple and its frequency response is relatively high. The circuit also has low input and high output impedances along with high current dynamic range and very low current transfer error. The simulation results are performed using

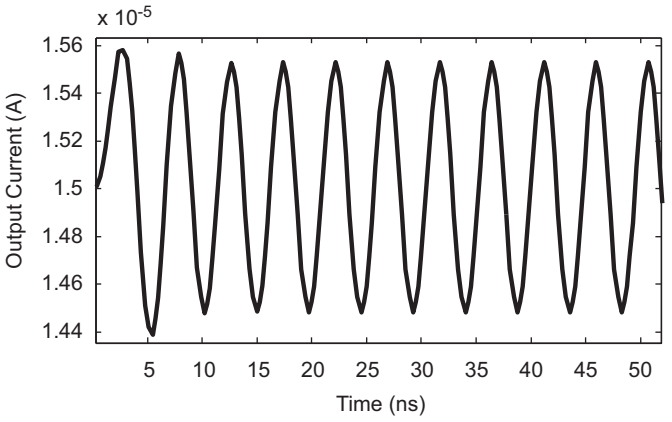

Fig. 16. Output current transient response applying sinusoid input current of $15u+1u\sin(2\pi\times 210\times 1E{+}6t)$.

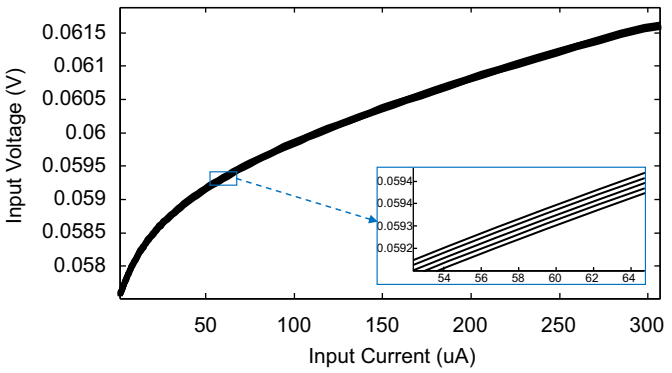

Fig. 17. Input voltage versus the input current applying ±10% variations in power supply voltage.

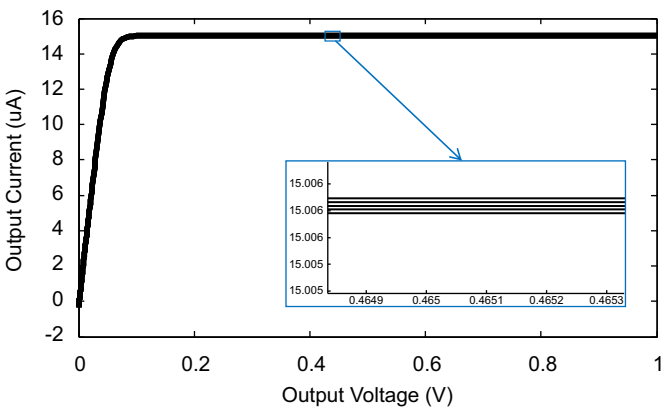

Fig. 18. Output current versus output voltage applying ±10% variations in power supply voltage.

HSPICETSMC 0.18 μm, BSIM3, Level49 and CMOS technologies using single 1 V power supply. The proposed current mirror is the best choice for low voltage, highly accurate and high output impedance applications.

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